Creation Of Sub-20nm Contact Using Diblock Copolymer With Conventional Lithography On A 300mm Wafer

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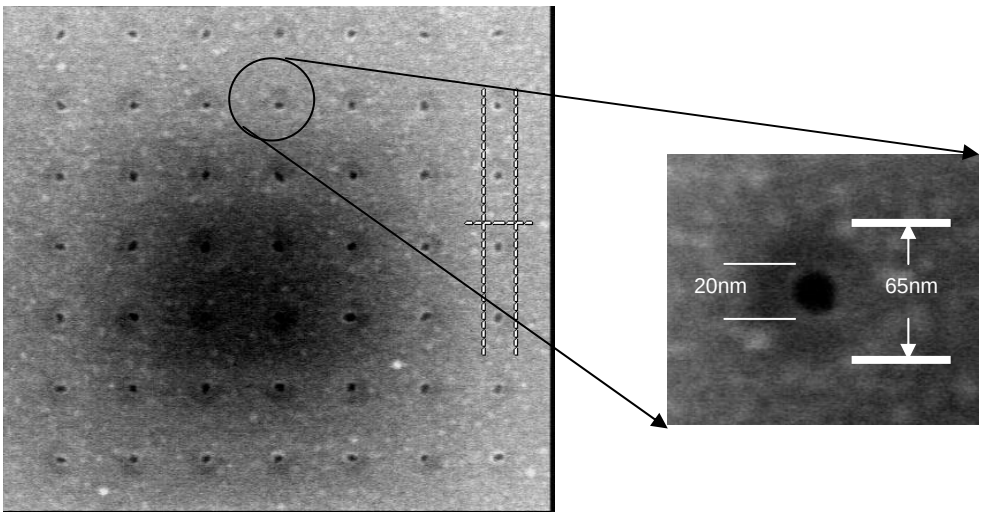
Development of block copolymers for next generation lithography provides an opportunity for researchers in developing future generation microprocessors. Many strategies to synthesize diblock copolymers for creating nanostructures such as dots and lines have been developed, for example nanocrytsal floating gate devices for FLASH memory fabrication1, and high-capacity metal oxide semiconductor capacitors2. Most semiconductor applications require the nanostructures be organized into precise locations. Therefore there is a need to develop a method for controlling the placement of these nanostructures.

In this paper, we will demonstrate a method to pattern sub 20nm dots of uniform size and location over a large area with cylinder-forming diblock copolymers. First a well is constructed using conventional lithography process. We call this well a "finite domain." The size of this finite domain determines the quantity of dots formed. For the case of one dot formed, each individual dot is created precisely at the center of the finite domain, and never on the edge or boundary. The number of dots is determined by domain size. The dot size, which can be as small as 10nm, can be adjusted by the molecular weight of the copolymer. This method is compatible with standard semiconductor processing techniques and can be applied to scaled contact holes required by 22nm VLSI technology node and beyond, we will discuss its application for forthcoming semiconductor manufacturing in details.

We have achieved sub 20nm dots over large areas that are well below photolithographic resolution limits and precisely registered in predicted locations. The dot size can be varied by different molecular weights of the PMMA and PS organic compounds. This method brings diblock polymer patterning techniques into the existing semiconductor process to realize contact hole dimension required by 22nm VLSI technology node.

Reference
(1) Guarini, K. W; Black, C. T.;Zhang, Y.; Babich, I. V.; Sikorski, E. M.;Gignac. L. M. Low voltage, Scalable Nanocrystal Flash Memory Fabrication by Templated Self-Assembly. IEDM 2003, IEEE International, NY,2003; pp22.2.1-22.2.4.
(2) Black C. T.;Guarini, K. W.; Milkove, K. R.; Baker, S. M.;Russell, T. P.;Tuominen, M.T. Appl. Phys. Lett 2001. 79,409-411



(a) SEM mircograph of precisely placed diblock copolymer dot patterns over on a 300mm wafer.

(b) Enlarged view of a single dot on top of the circular finite domain.