EUV Lithography at IMEC

<u>G. F. Lorusso</u>, A. M. Goethals, R. Jonckheere, J. Hermans, and K. Ronse *IMEC, Kapeldreef 75, B-3001 Leuven, Belgium* A. M. Myers *Intel Corporation, 2200 Mission College Boulevard, Santa Clara CA 95054* I. Kim *Samsung Electronics San #24 Nongseo-Dong Giheung-Gu, Yongin-City Gyeonggi-Do, 499-711 Korea* A. Niroomand *Micron Technology, MS 1-717, 8000 S. Federal Way, Boise, ID 83716* F. Iwamoto *Matsushita, 1 Kotari-yakemachi, Nagaokakyou, Kyoto* D. Ritter *SIGMA-C Software AG, Thomas-Dehler-Str. 9, D-81737 Munich, Germany*

There is widespread industry consensus that Extreme Ultraviolet Lithography (EUVL) is the leading candidate for the 22 nm node and beyond. By installing the world's first EUV full-field scanner (Fig. 1), IMEC now has a fullyintegrated, 300mm process line capable of properly investigating EUVL readiness for high-volume manufacturing (HVM). In particular, topics such as flare (caused by light scattered by roughness in the optics) and shadowing (consequence of the surface topography of multilayer masks) are now added to the list of the development requirements in need of understanding, quantification and ultimately mitigation. EUV resist has to satisfy simultaneously resolution, dose, and LER requirements, and screening requires interference lithography (Fig. 2) or EUV scanners. In addition, its qualification in terms of outgassing needs new methodologies in order to prevent the contamination of the multilayer optics. Availability of defect-free reticle handling and protection during storage and use in the absence of a conventional pellicle is another critical challenge for EUVL.

In this paper, we will present our progress in various EUVL-specific areas. The focus will be on imaging, flare, shadowing, EUV resist, and multilayer mask. The status of the EUV ADT will be reviewed and first imaging performance will be discussed. Extensive simulation work on all topics will be presented, as well as results of EUV resist screenings carried out using EUV interference lithography at synchrotron facilities.



Fig 1: ASML EUV Alpha Demo Tool at IMEC.



Fig 2: EUV resist showing resolution down to 30nm L/S obtained with EUV interference lithography.