Patterned Wafer Defect Density Analysis of Step and Flash Imprint Lithography

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Imprint lithography has been shown to be an effective method for the replication of nanometer-scale structures from a template mold.[1] Step and Flash Imprint Lithography (S-FIL^{TM}) is unique in its ability to address both resolution and alignment. Recently overlay across a 200 mm wafer of less than 20nm, 3σ has been demonstrated.[2] These results motivate the consideration of nano-imprint lithography as an NGL solution for IC production. However, CMOS manufacturers well understand that the commercial viability of a production process also depends on limiting the accumulation of defects. During the Step and Flash Imprint Lithography process, a transferable image, an imprint, is produced by mechanically molding a liquid UV-curable resist on a wafer. The novelty of this process immediately raises questions about the overall defectivity level of SFIL. Acceptance of imprint lithography for CMOS manufacturing will require demonstration that it can attain defect levels commensurate with the requirements of cost-effective device production.

This presentation will summarize the result of a comprehensive defect inspection of wafers patterned using S-FIL. The mask or templates used to imprint wafers for this study were designed specifically to facilitate automated defect inspection. The templates were made by employing CMOS industry standard materials and exposure tools. The method for fabricating the template used in this study is outlined in Figure 1a. Two patterns, a Metal 1 array and an SRAM contact array were targeted for inspection. The primary wafer inspection was performed using a KLA-2132 automated patterned wafer inspection tool. Additional inspections were carried out on a high-resolution scanning-electron-beam inspection tool. The resolution of the KLA-2132 is limited to approximately 200 nm and the high resolution tools were employed to further extend the solution of defect capture to 25 nm. Defects were reviewed on a JEOL review SEM, and with additional optical tools. The inspection results show that the defect density of imprinted wafers is determined by contamination of the wafer or template.

An example of a fully inspected wafer is shown in Figures 2a and 2b. Figure 2a depicts a defect map which includes both the repeating and random defects detected. For this particular sample, approximately 5 defects resulting from the fabrication process caused repeating defects. Figure 2b depicts a Pareto of the detected defects. There were very few (1.2 cm-2) random defect events. Figure 3a depicts an early imprint in which a large particle was encountered. Contamination of the template (shown in a subsequent imprint (Figure 3b)) was minimal. The result of automated inspection of template and correlation of template defects with imprints will be discussed. The paper will also cover the potential sources for defects.

1. F. Hua, et al., Nano Lett. **4**(12), 2467-2471 (2004).
2. P. Schumaker et al., presented at SPIE Microlithography 2006, Emerging Lithographic Technologies X.

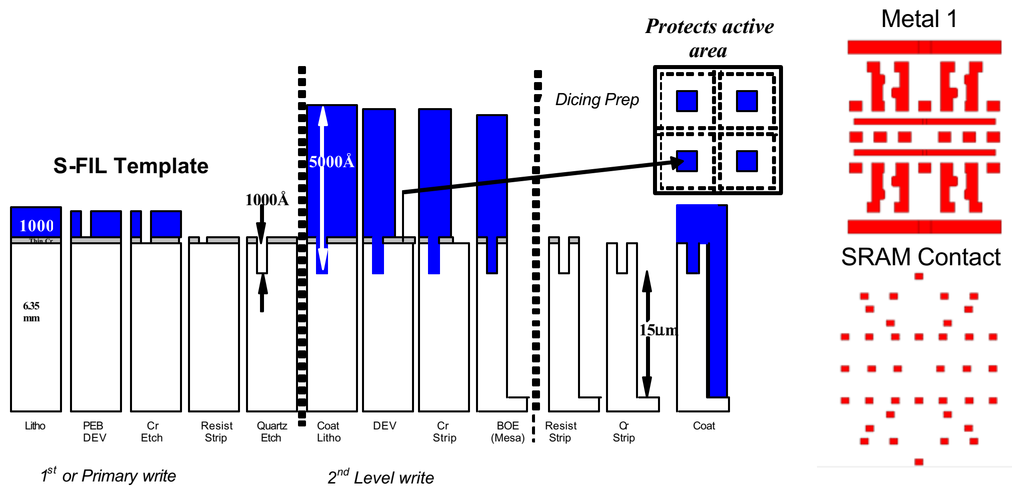

Figure 1. a) Template fabrication process. b) SRAM contact and Metal 1 array patterns used to evaluate defectivity.

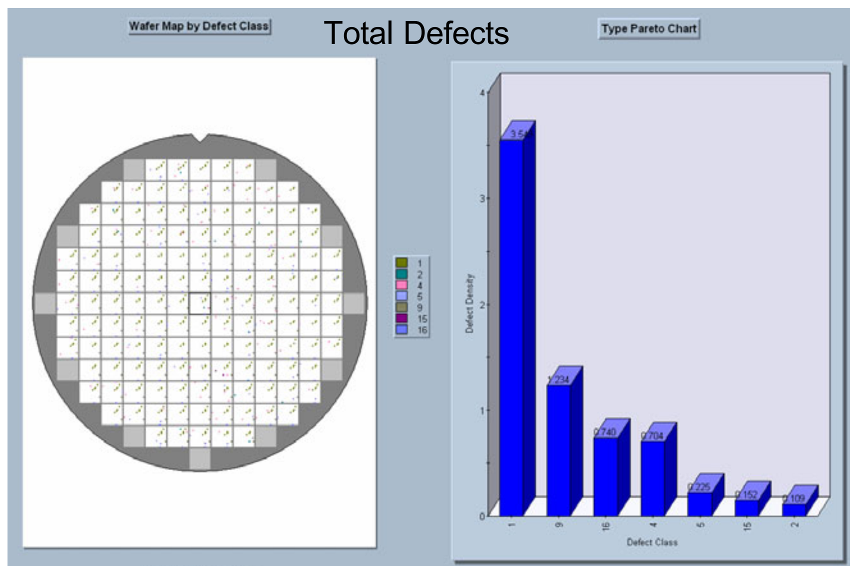

Figure 2. a) Total defect map across the imprinted wafer. b) Total defect density Pareto. The total defect density is 6.7 cm-2. The random defect density is 1.2 cm-2.

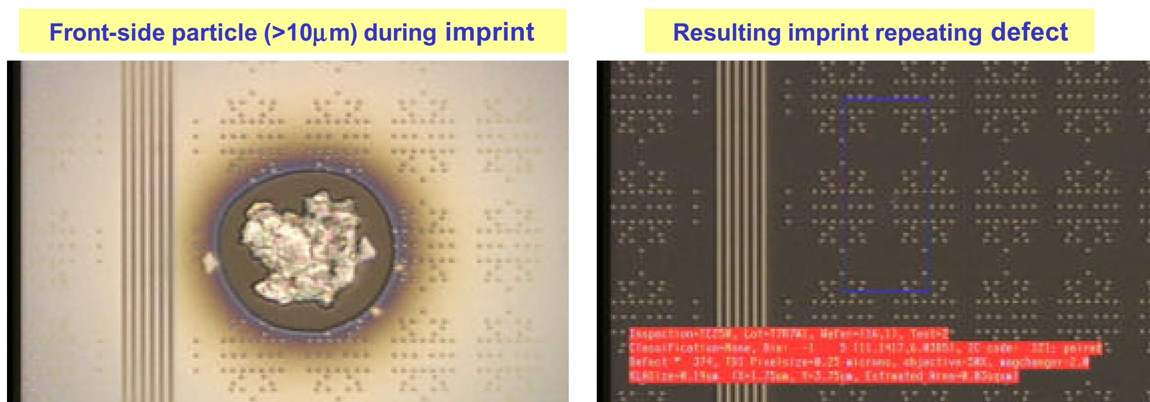

Figure 3. a) Front side particle encountered during the initial imprint process. b) The contamination resulting from this particular defect.