Highly Scalable Resistance-Change Memory

Michael N. Kozicki
Center for Applied Nanoionics
Arizona State University
Tempe, Arizona 85287-6206, USA

The challenges associated with the scaling of conventional non-volatile memory devices have resulted in the development of a multitude of new technologies. The most promising category does not rely on charge storage, which leads to problems of sensing and retention in highly-scaled structures, but instead uses a change in resistance to represent stored data. Whereas several resistance-change technologies have captured the interest of the industry, most lack *complete* scalability as they require programming voltage or current that is excessive for high density integrated systems beyond the 32 nm node of the International Technology Roadmap for Semiconductors. A potential solution to this quandary involves the use of solid electrolyte films. One example utilizes a silver or copper ion-containing electrolyte film sandwiched between a silver/copper layer and an inert electrode. This constitutes a device which may be rapidly switched from a high to a low resistance by the formation of a nanoscale conducting bridge created by reduction of the metal ions. A reverse bias dissolves the connection. This reversible switching between widely-spaced resistance states is attainable even for voltages of a few hundred mV and currents in the μA range. Such devices therefore have excellent scaling prospects due to their low operational energy in addition to their demonstrated physical scalability.

Our own resistance-change variant, Programmable Metallization Cell (PMC), uses a thin film of Cu- or Ag-doped Ge-Se, Ge-S, WO_3, or SiO_2 between two electrodes; Cu or Ag is used as an oxidizable electrode on the electrolyte and the lower electrode can be the W via plug in a standard CMOS process. In the case of the Cu-SiO_2 electrolyte, integration is particularly simple as both copper and silicon dioxide are present in back-end-of-line processing schemes. The on-state resistance, which is typically more than four orders of magnitude lower than the off-state, is defined by the programming current limit which facilitates multi-level cell (MLC) operation. Retention is excellent with over ten years demonstrated at elevated temperature and devices have been cycled in the low current range (a few tens of μA and below) to well beyond 10^{12} cycles. Write and erase times within 20 ns have been attained for the high ion mobility electrolytes.

This presentation will review solid electrolyte resistance-change devices and will discuss how the electrical characteristics of the most promising variants could be ideal for future low power, high density memory and storage applications.