# A Novel 3D Lithography: Self Aligned Patterning Through Thin Layers

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The first 3D lithography through silicon layer is reported here. High energy electron beam lithography (EBL) has been performed from side to side of a planar thin silicon layer. This results with self aligned patterns [1]. Applications are discussed.

Test structures have been developed using the scheme described here. Monocrystal SiGe/Si bilayer is grown on a full sheet wafer. Standard lithography and anisotropic etch is performed to open laterally on SiGe. Thus this layer can be partially etched, selectively versus silicon using CF4 plasma, (SON process [2]). This results with a silicon bridge over SiGe pillar (fig 1). Lithographic sequence is then described fig2: Resist is spin coated, we perform electron exposure using Leica (Vistec) VB6HR tool at 50keV, and development. Thanks to high energy exposure, electrons are able to expose same pattern on both sides of a thin silicon layer. Demonstration is done with a 100 nm width TEM sample, cut in the silicon bridge, using HSQ $(HSiO_{3/2})_{2n}$ resist (fig3). The silicon thickness is 29nm, top CD is 79nm, bottom CD is 106nm. Oxygen map points out HSQ pattern on both side of the silicon layer (fig3). Experiments have been associated with simulation. Stack and electron exposure are simulated using SELID simulator (fig4). No major beam deviation is observed. Therefore we think CD control could be increased thanks to development step optimization.

Considering its resolution potential, this process can be applied to CMOS innovative architecture. Indeed one of the great challenges for the planar double gate integration (one of best candidate for ultimate technological nodes) is the self alignment of top and bottom gates. A few papers demonstrated the feasibility, or with complex integration [3][4]. HSQ is a spin coatable oxide which is also a negative tone electron beam resist. During curing, or electron exposure, its cage-like structure $(HSiO_{3/2})_{2n}$ is opened, and forms a network structure [5]. It leads to a low-k dielectric, similar to $SiO_2$. Thus HSQ resist can be part of a front end process. HSQ patterns shown before being considered as a template for top and bottom gates, we demonstrate a revolutionary way to integrate self-aligned planar double gate transistor.

[1] US patent *2005/0037603 A1* [2] : Borel et al., ECS Transactions 3(7), 627-642 (2006) [3] Lee et al., VLSI Tech. Dig. 2005 pp154-155 [4] Wacquez et al., SSDM 2006, pp534-535. [5] Liou et al., Thin Solid Films 335 (1998) 186-191

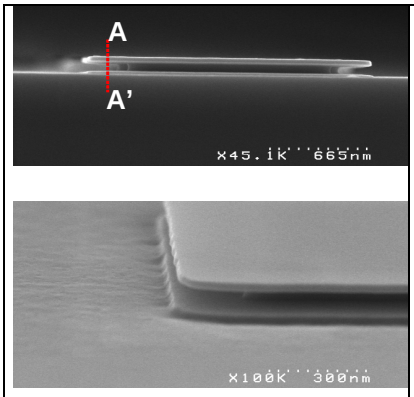



Fig.1 SEM view of our test structure: monocrystalline silicon layer over monocrystalline SiGe pillar.

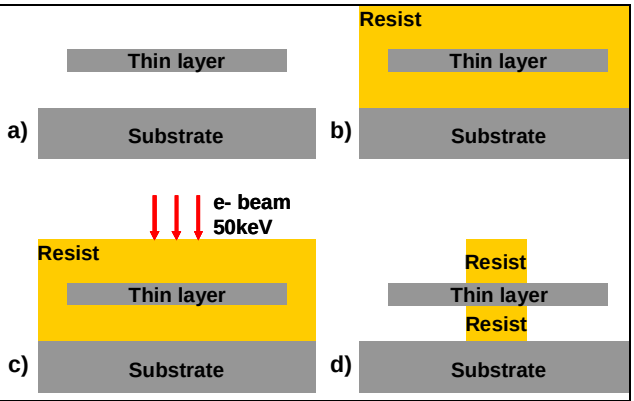
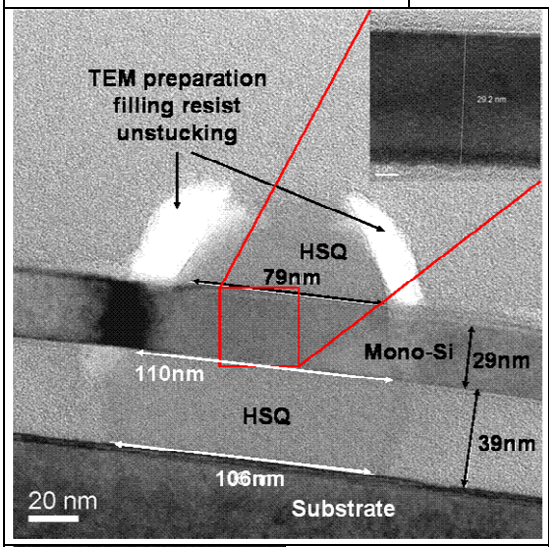



Fig.2 : Main steps of 3D lithography (AA' cut, see Fig.1) a) a thin layer (Si, SiGe etc …) bridge is created. b) Resist is spin coated, over and under the bridge. c) Standard High energy e-beam is performed. d) Development is done..



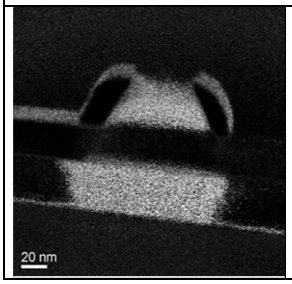




Fig.3 : Final structure TEM view.
Insert is monocrystalline silicon magnification.
Left is oxygen map of the structure.

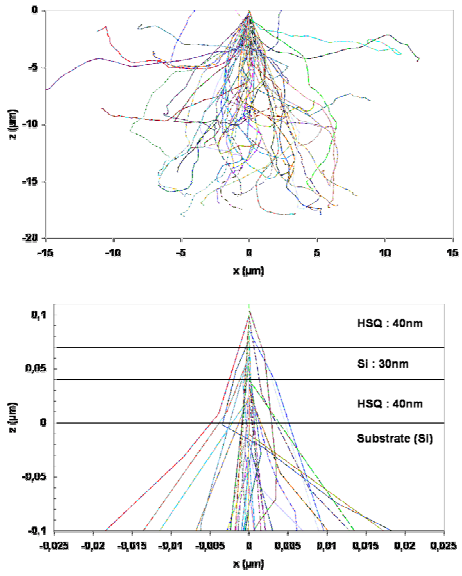



Fig.4 : Electron exposure Monte Carlo simulation (SELID). Stack corresponds to experience (fig.3), beam energy is 50keV.