Hybrid Carbon Nanotube-Silicon CMOS Circuits

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With the semiconductor industry facing increasing challenges in scaling silicon devices to smaller dimensions, there is particular interest in the remarkable electronic properties of carbon nanotubes (CNTs), which are currently considered by some as a possible alternative to silicon for future nanoelectronics applications. Steady improvements have been achieved in carbon nanotube field-effect transistor (CNFET) performance, and it has already been demonstrated that the intrinsic current carrying capabilities of carbon nanotubes exceed those of silicon.[1,2] Along with progress in optimizing the structure and performance of individual CNFETs, some simple CNT-based circuits have recently been reported toward the goal of high frequency CNT electronics.[3]

The most likely early implementations of CNT-based electronics would involve the integration of CNFETs with existing silicon technology infrastructure. In a previous demonstration of combined CNFET and Si NMOS transistor circuits[4] the Si transistors were used only as decoders to address the CNFETs. True hybrid circuits, on the other hand, would likely comprise arrays of high-performance CNFETs designed for specific low-fanout logic functions which interface with conventional Si CMOS when higher current drive is required. We have developed a CNFET process that can be applied on the back end of a commercial submicron CMOS chip. The fabrication involves a transfer mechanism[5] that allows carbon nanotubes to be grown at high temperature before being placed with lithographic precision onto the Si CMOS chip, resulting in three-dimensional integration of Si and CNFET devices interconnected through the second metal wiring layer of the Si chip.

CNTs are grown from Co/Mo catalyst by CVD suspended across a ~ 100 μm-wide slit in a Si wafer. The suspended tubes are characterized by Raman and Rayleigh scattering to determine their chiral indices (and whether they are semiconducting or metallic). They are then transferred onto a foundry-fabricated 0.25 μm Si CMOS chip in a mask aligner by embedding the suspended tubes in photoresist and releasing them from the original growth substrate. Electron beam lithography defines multi-fingered source and drain contacts as well as interconnects to the underlying Si devices, forming a hybrid CNT/Si CMOS inverter. Metal gates are defined on the CNTs using atomic layer deposited Al_2O_3 or HfO_2 as dielectrics. Figure 1 shows a schematic of the hybrid chip (a), along with an image of a completed hybrid circuit (b) and an image of the transferred CNT following the transfer process (c). Preliminary electrical characteristics are shown in Fig. 2.

We will present details of the complete fabrication process, from CNT growth to CMOS integration, along with electrical results and a description of a self-aligned CNFET process designed for optimal performance at high frequency.

[1] S. J. Wind, J. Appenzeller, R. Martel, V. Derycke, and Ph. Avouris, Appl. Phys. Lett. **80**, 3817 (2002).
[2]A. Javey, J. Guo, Q. Wang, M. Lundstrom, and H. Dai, Nature **424**, 654 (2003).
[3] Z. Chen, J. Appenzeller, Y. Lin, J. Sippel-Oakley, A. G. Rinzler, J. Tang, S. J. Wind, P. M. Solomon, and P. Avouris, Science **311**, 1735(2006).
[4] Y.-C. Tseng, P. Xuan, A. Javey, R. Malloy, Q. Wang, J. Bokor, and H. Dai, Nano Lett. **4**, 123 (2004).
[5]X. M. H. Huang, R. Caldwell, L. Huang, S. C. Jun, M. Huang, M. Y. Sfeir, S. P. O'Brien, and J. Hone, Nano Lett. **5**, 1515 (2005).

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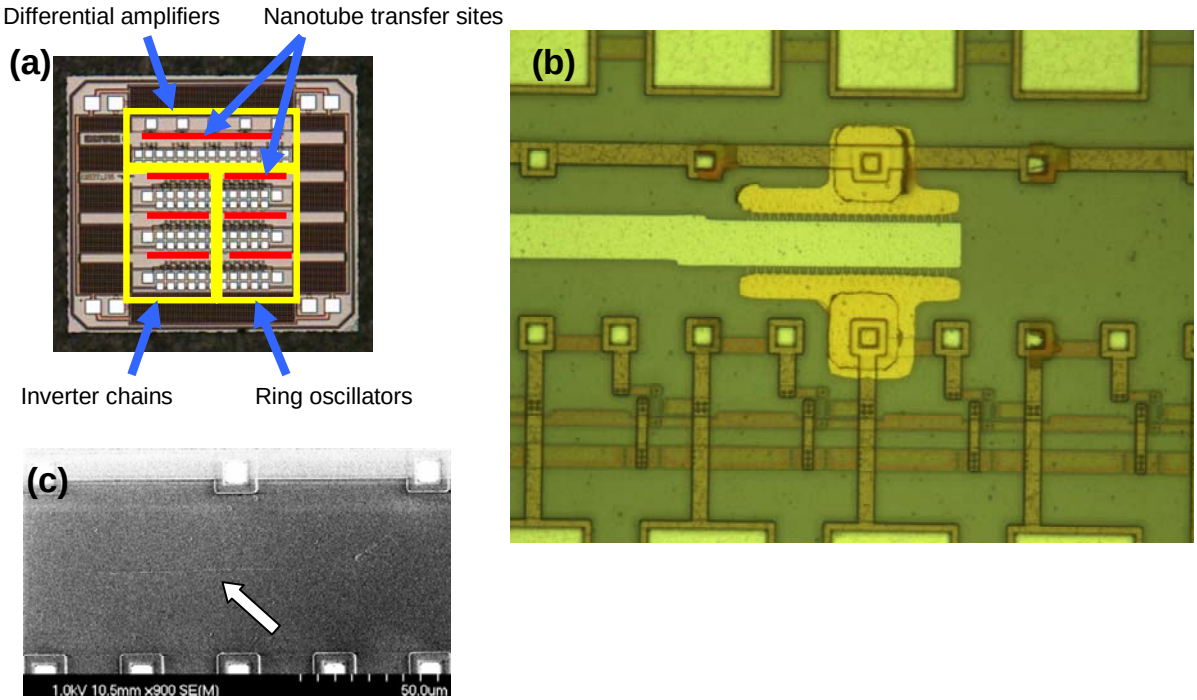

Figure 1. (a) Image of CMOS substrate overlayed with the site for nanotube transfer for hybrid circuit fabrication. (b) Fabricated CNFET pFET device. (c) SEM micrograph of transferred nanotube (noted with arrow) before device fabrication.

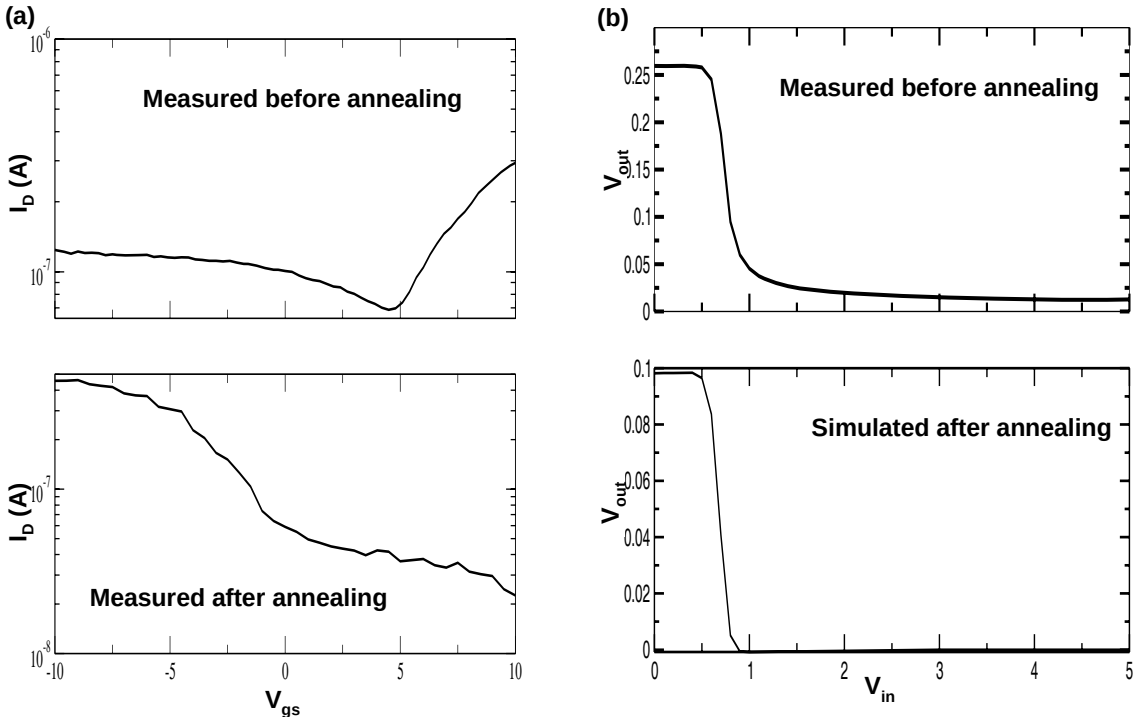

Figure 2. (a) CNFET transfer characteristics measured before and after annealing. (b) Hybrid CNT/Si inverter voltage transfer curve before (measured) and after (simulated) annealing.