Novel Coexisted Sol-Gel Derived SONOS-Type Memory

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Thin film and nanocrystal based materials have recently attracted much more attention for the application in the next-generation nonvolatile memories. Recently, numerous novel technologies such as PVD, CVD and ALD have been developed for the nanocrystal memory. The sol-gel method is also an alternative candidate to fabricate the SONOS type memory. The formation of thin film and array nanocrystal with sol-gel spin coating is a very simple method due to its cheaper precursor and tool. In addition, the film can be fabricated in the normal pressure system instead of expensive high vacuum system.

In this work, we propose the thin film and nanocrystal devices with sol-gel solution as a basis for the SONOS-type memories. Except for the sol-gel spin coating, the memory device is fabricated by the conventional CMOS nanofabrication in Fig. 1. Figure 2 shows the Id-Vg curves for the SONOS-type memories fabricated by the 10nm HfO_2 thin film, one type of nanocrystal, and two types of coexisted nanocrystals, respectively. The program condition is operated at Vg = 15V and Vd = 10V for 10 msec. The erase condition is operated at Vg = -10V and Vd = 10V for 1 sec. The obtained memory window from Fig. 2 is 3V, 3.3V, and 4V for these memories. We find the two types of coexisted nanocrystals exhibits better performance than other types. This observation is attributed to the more charge trapping sites. Gate disturbance for these memories is illustrated in Figures 3(a-c). We measure the erased state devices under Vg=10V or 12V. From these figures, the thin film based memory exhibits the unsatisfactory result on gate disturbance. However, the nanocrystal based memory demonstrates the tolerant effect on gate disturbance. In addition, the read disturbance in Figures 3(d-f) also supports the performance enhancement effect of nanocrystal based memory. The improvement of tolerant effect on gate or read disturbance is related to the increase of the equivalent tunneling oxide thickness. More results of memory characterization will be presented in the conference.

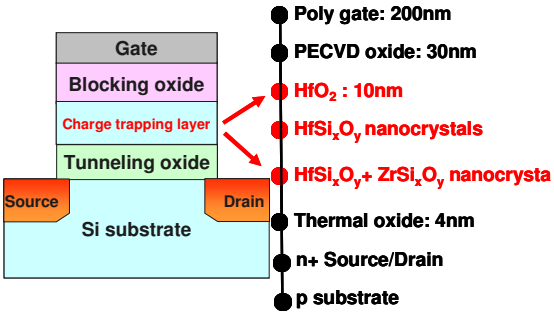

Figure 1. Schematic diagram of the device structure for the spin coating charge trapping film and nanocrystal memories.

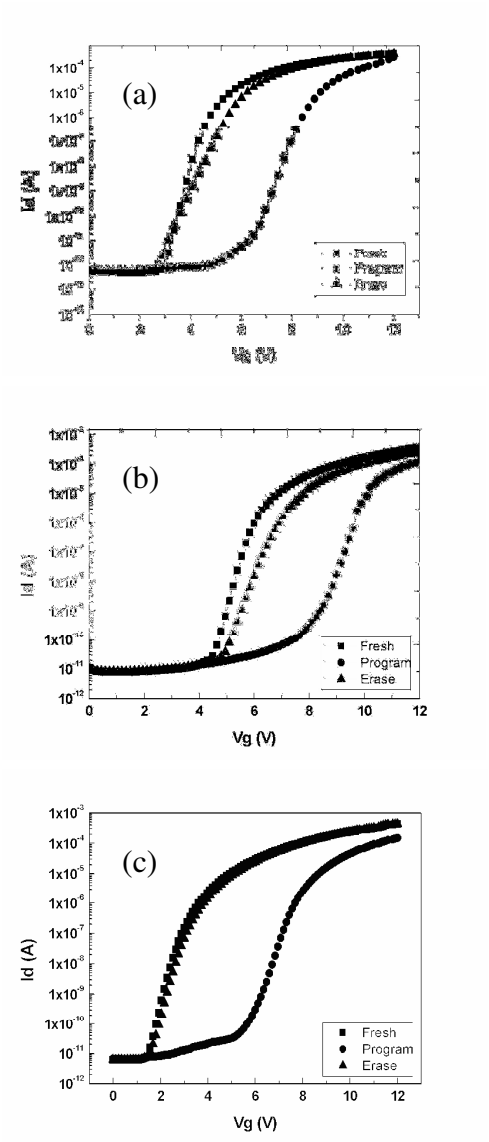

Figure 2. The Id-Vg curve of SONOS-type memories: (a) 10nm HfO_2 thin film, (b) $HfSi_xO_y$ array nanocrystals, and (c) $HfSi_xO_y$ and $ZrSi_xO_y$ array nanocrystals.

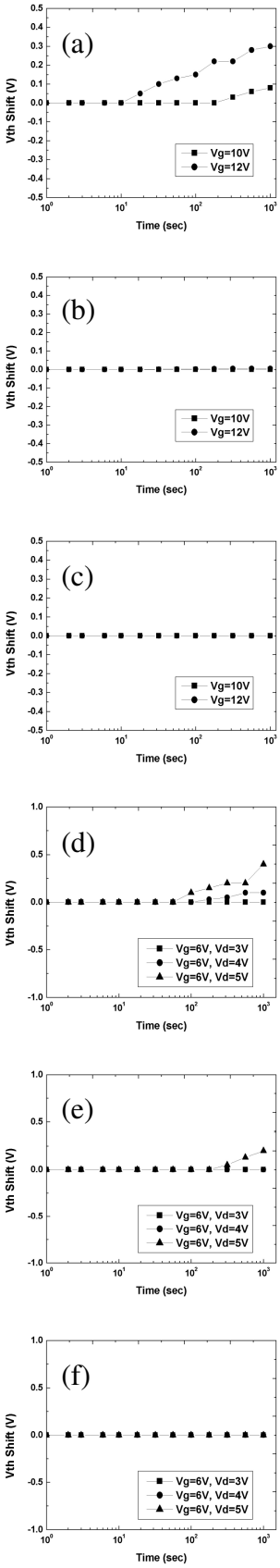

Figure 3. Gate disturbance of (a) 10nm HfO_2 thin film, (b) $HfSi_xO_y$ array nanocrystals, and (c) $HfSi_xO_y$ and $ZrSi_xO_y$ array nanocrystals; read disturbance of (d) 10nm HfO_2 thin film, (e) $HfSi_xO_y$ array nanocrystals, and (f) $HfSi_xO_y$ and $ZrSi_xO_y$ array nanocrystals.