Adaptive wiring for 20 nm scale epitaxial silicon ohmic contacts to silicon nanowires

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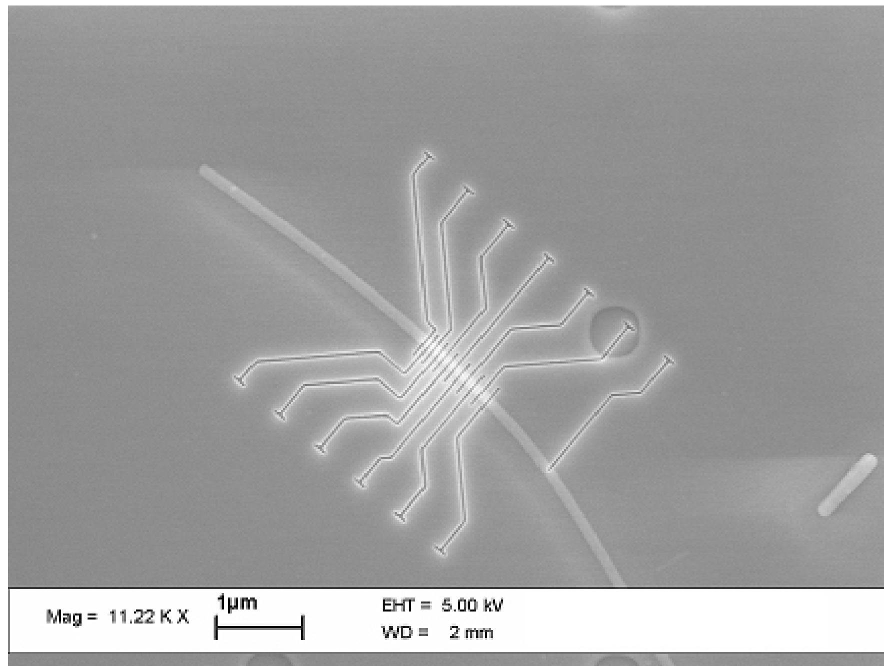
We report techniques for the fabrication of closely-spaced contacts to silicon nanowires. The random placement of nanowires on the substrates requires wiring which is adapted to each individual target nanowire. Electron-beam lithography is used to define 20 nm scale contacts, and the versatility of e-beam allows optimization of wiring translation and rotation at the time of pattern exposure. We also make use of an alternative technique wherein a large array of contact lines and pads are printed without alignment to individual nanowires. In this case nanowires are connected by chance, relying on relatively long contact lines with relatively large spacing (down to 200 nm). We compare the advantages of the two wiring techniques.

Contacts to silicon nanowires are formed by etching holes through a dielectric stack of silicon dioxide and silicon nitride. P-type, in-situ doped epitaxial silicon is grown through the holes, then polished flat to form wires. The process is similar to forming a raised source/drain on conventional FETs, but in this case the contacts are much smaller and epitaxial growth is from a cylindrical substrate. Nickel, and optionally nickel silicide, is used to complete connections to probe pads. Electrical measurements using epitaxial contacts are compared to those using metal (Ni) Schottky contacts. The nanowires in this study are not intentionally doped, but are gated through the substrate. Measurements show that the ambipolar characteristics induced by Schottky contacts have been eliminated through the use of in-situ doped epitaxial silicon contacts. N-type contacts have also been fabricated on larger, 0.5 μm scale contact holes, using a combination of P and As implantation.

(a)



(b)

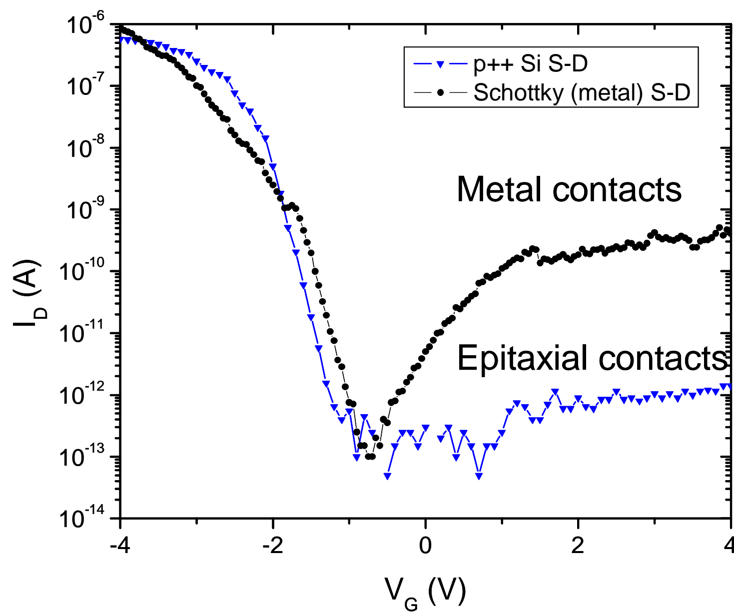


Figure: (a) Contact holes etched through silicon nitride to a silicon nanowire. The holes will be filled with epitaxial and poly silicon, then connected to probe pads with Ni lines. (b) Drain current vs. gate voltage measured for nanowire FETs having a diameter of 25 nm, a 400 nm long gate and source-drain contacts of either metal (circles) or p-type doped silicon (triangles). The wires are back-gated.