Progress towards gate alignment for atomically precise STM-patterned devices

M. Fuechsle [1, 2], F. J. Rueß [1, 2], T.C.G. Reusch[1, 2], M. Mitic[1, 2], and M. Y. Simmons [1, 2]

1. Centre for Quantum Computer Technology, University of New South Wales, Sydney New South Wales 2052, Australia
2. School of Physics, University of New South Wales, Sydney, Sydney, New South Wales 2052, Australia

The capability of the scanning tunnelling microscope (STM) to perform nanolithography on hydrogen-passivated silicon surfaces has allowed the fabrication of atomically precise, planar, highly phosphorous-doped devices in Si [1-4]. Electrical characterisation of these atomic-scale devices requires *ex-situ* registration of macroscopic contacts to the buried STM-patterned device layers [3]. Several strategies have been developed to align external contacts to STM-patterned regions including prepatterning the initial silicon substrate with registration markers by means of optical or electron beam lithography (EBL) and/or subsequent metal deposition [5], ion implantation [2], or etching [3]. However, the need for a high temperature anneal (flashing) to prepare the Si substrate for STM-lithography limits the practicability of using metal deposition or implantation due to the possible diffusion of impurities to the device region.

We have developed a complete, fully EBL-based fabrication scheme for aligning multi-terminal ohmic contacts and gates to STM-patterned, buried P-doped nanostructures on the Si(100) surface using etched markers. Furthermore, we have investigated how to create atomically flat, step-free device regions on the Si(100) substrate so the active region of the device can be patterned on a single atomic plane. A hierarchic array of EBL-defined registration markers is wet chemically etched into the Si(100) substrate (Fig. 1). These markers are fully compatible with the ultra high vacuum (UHV) environment and survive the required flashing at ~1100°C to reconstruct the surface. A central circular trench defines the device region, which due to a step-bunching process during flashing forms an atomically flat terrace exactly in the centre (Fig. 2). After STM-lithography, dopant incorporation, and encapsulation with epitaxial Si, the sample is taken out of the UHV system and ohmic contacts and gates are EBL-patterned and metallized (Fig. 3) with respect to these initial markers.

The current overall alignment accuracy of ~100 nm is limited only by the rounding of the etched marker edges during flashing and Si overgrowth, causing inaccuracy in the subsequent EBL alignment step. However, we are confident that this accuracy can be improved by incorporating etched Moiré-type gratings into our current alignment scheme.

[1] Ruess, F.J., *et al*., *Nano Letters* **4**, 1969 (2004)
[2] Shen, T.C., *et al*., *J. Vac. Sci. Technol. B* **22**, 3182 (2004)
[3] Ruess, F.J., *et al*., *Nanotechnology* **16**, 2446 (2005)
[4] Ruess, F.J., *et al., Nanotechnology* **18,** 044023 (2007)
[5] Fujimori, M, *et al*., *Nanotechnology* **15**, S333 (2004)

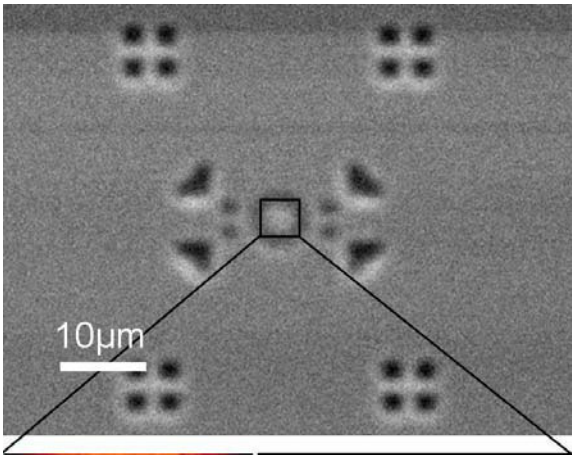

Fig. 1: SEM image of the etched registration markers on Si(100) after STM sample preparation at 1100°C for 1min. The central circular trench defines the active device region.

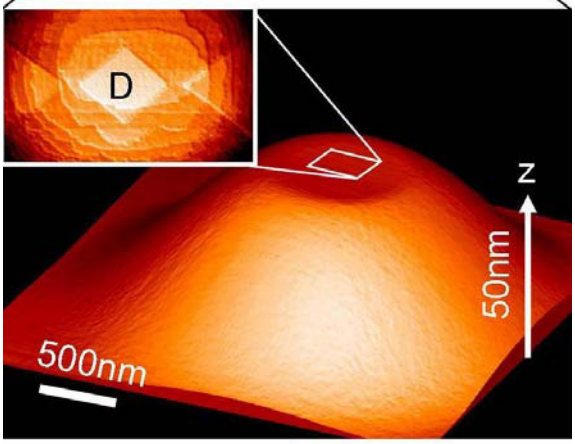

Fig. 2: STM image of the central device region. An atomically flat terrace is formed in the middle of the circular marker (image not to scale z-direction).
Inset: STM-patterned quantum dot in the central region on a hydrogen-passivated Si surface before dopant incorporation. The width of the diamond-shaped dot (D) is 270nm.

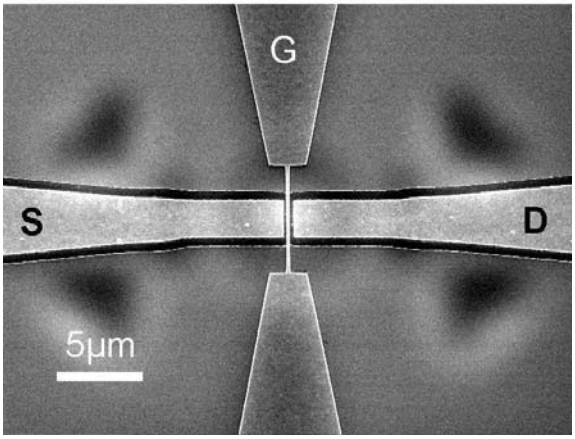

Fig. 3: An SEM image showing EBL-patterned ohmic contacts (S,D) and a 150nm central gate (G) aligned to the registration markers and the central terrace after metallization.