Study of process contributions to total overlay error budget for sub 60 nm memory devices

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According to the international technology roadmap for semiconductor 2005, overlay budget of 60 nm node flash memory device is around 12 nm. Within a few years, it needs to be kept less than 10 nm. To meet such a tight requirement, total overlay error budget should be controlled carefully. There are many ways to analyze overlay budget. In this study, however, the most simple but accurate methodology is introduced as followings. It is assumed that total overlay error budget consists of four major parts. Those are scanner, process, metrology, and mask. Scanner contributions present machine to machine overlay error. Process contributions are mainly due to photolithography, dry etch, and chemical mechanical polishing (CMP). Metrology contributions are from align/overlay metrology tools. Finally, mask contributions present mask to mask mis-registration during electron beam writing. By applying this methodology to 60 nm node memory devices, it turns out that process contributions are nearly half of total overlay error budget. In this paper, optimum process widow is investigated so that process effects such as inverse reactive ion etching lag and CMP erosion can be minimized. In photolithography process, wafer stack is optimized so that the image quality of align/overlay mark is robust to the process variations. By integrating the optimized process window, overlay budget is confirmed for sub 60 nm memory devices.

Key words: semiconductor, photolithography, overlay, alignment

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