Fabrication of dense sub-20nm pillar arrays on fused silica imprint templates

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A number of emerging applications have demonstrated the need for a practical manufacturing process capable of patterning large-area arrays of dense sub-50nm structures. These applications range from patterned magnetic media for high-density data storage to ultra-sensitive biological sensors based on surface-enhanced Raman scattering. Such concepts have been proven in research labs using direct-write electron beam lithography, but this patterning approach is much too slow to be feasible as a mass-production solution. Imprint lithography is an effective method for accurate replication of nanostructures from a patterned mold; Step and Flash Imprint Lithography (S-FIL™) has been demonstrated as a high-throughput approach to imprint patterning with a thin, uniform residual layer. S-FIL employs a fused silica imprint template that can be patterned by direct writing with an electron beam; this template can then be replicated thousands of times in the high-throughput imprint process. S-FIL can be incorporated into a variety of manufacturing process flows, including lift-off patterning, dry etch transfer into the underlying substrate, electroplating, and direct patterning of a functional imprint material.

The objective of this work is to create fused silica templates for imprint patterning of magnetic media. This application requires precise placement of sub-20nm pillars in dense arrays that cover many square centimeters. Several electron-beam resist materials are known to be capable of resolving dense sub-20nm structures, but only a few of these are practical for patterning large areas. In this study, poly(methyl methacrylate) (PMMA) and ZEP520A (Zeon Corporation) are implemented in a lift-off process to produce dense arrays of Cr dots. Prior to resist coating, a thin metallic layer is evaporated on the fused silica substrate to provide electrical conductivity during electron beam exposure. Resist films are 45nm in thickness and electron-beam exposures are performed on a 100kV Vistec VB6HR exposure system. Resist development, descum etching, and lift-off conditions are selected and systematically optimized to identify a process window for patterning sub-20nm half-pitch Cr dot arrays over large areas with minimal defectivity. This paper describes the optimization of the lift-off process, which is generally applicable beyond imprint template fabrication. Top-down SEM images of Cr dot arrays are shown in Fig. 1. In the final step of template fabrication, the Cr dot pattern is transferred into the underlying fused silica substrate with a fluorocarbon dry etch process, producing the topography seen in the tilt-SEM image in Fig. 2. This pattern can be accurately replicated through the S-FIL process, as shown in Fig. 3.

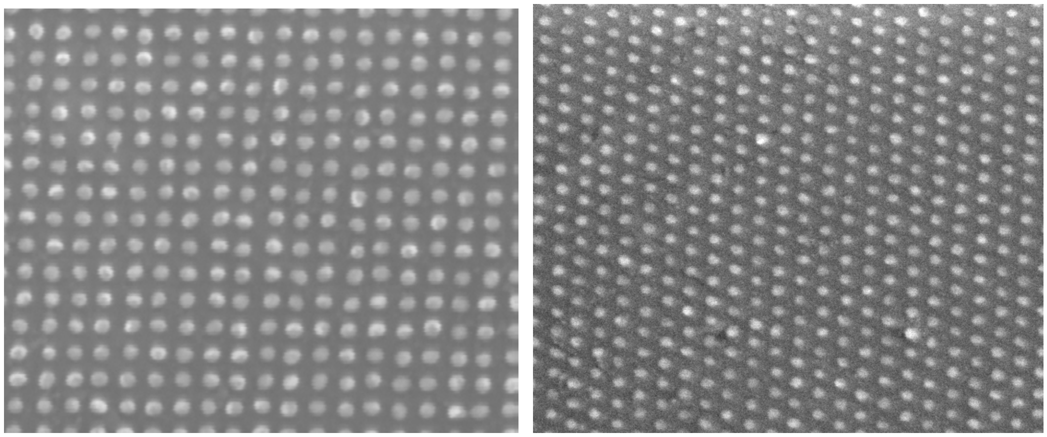

Figure 1. 19nm half-pitch Cr dots in (a) square and (b) staggered arrays.

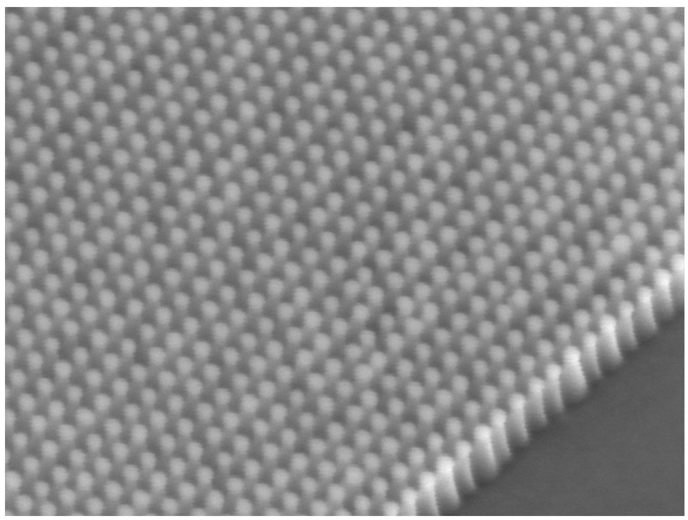

Figure 2. 21nm half-pitch pillars etched 80nm into fused silica.

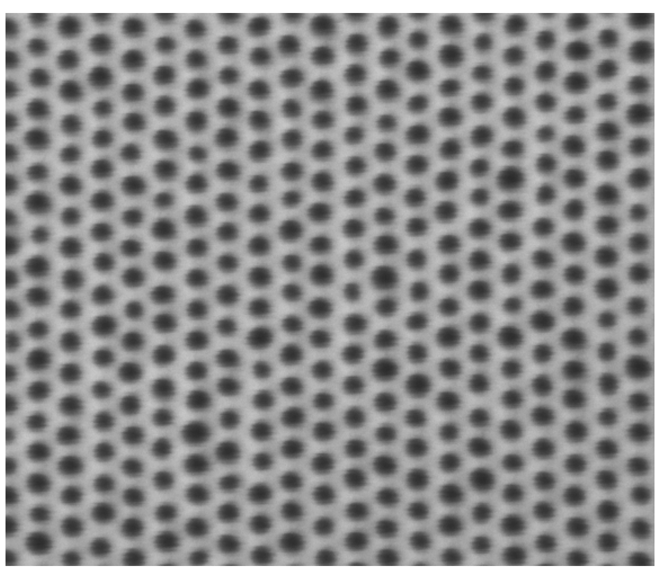

Figure 3. Imprinted 21nm half-pitch array of staggered holes.