Line Edge Roughness Impact on Critical Dimension Uniformity and Device Performance for sub-32 nm Technology

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Critical dimension (CD) control is one of the key requirements for manufacturing integrated circuits. For the 32 nm node, the 2005 International Technology Roadmap for Semiconductor (ITRS)[1] specifies a resist requirement for gate resolution and gate CD control (3σ) of 1.3 nm. However, CD uniformity control becomes more and more statistically limited with the continuous aggressive technology scaling. In this paper, we will present a fundamental study of the line edge roughness (LER) effect on CD variation across the wafer and on the electrical performance of the devices for sub-32nm technology.

The power spectral density (PSD), which is a function of roughness σ, correlation length L_c, and fractal dimension, is usually used to simulate the LER[2,3]. In our study, for a given gate width, we generated more than 10^4 line edges with PSD with specified LER, L_c, and fractal dimension. The simulated line edges are then input into HSPICE in order to check the LER impact on the electrical characteristics of devices such as drive current, leakage current and threshold voltage.

It is shown that the CD variation not only depends on the LER, but also on L_c. The larger the L_c, the more CD variation across the chip will be. The relationship between CD variation and L_c could become exponential as the gate width scales comparably to L_c. Figure 1 shows how the CD variation and the contribution of CD variation from lithography process vary with L_c at $3\sigma = 4nm$, the gate width W=50 nm and the gate length of 30 nm. It is shown that 70% of the CD variation could come from the lithography process if the final L_c is larger than 5 nm under the assumption that the final L_c of line edges is twice that of L_c from lithography. Figure 2 shows the preliminary HSPICE simulation results for the drain saturation current distribution and the threshold voltage distribution with $3\sigma = 4nm$ at Lc=25nm. It is shown that the 36mV-variation (3σ) of the threshold voltage is induced purely from the line edge roughness of individual gates, and as a result, 5% (3σ) of the absolute saturation drain current distribution occurs with the metric of σ/μ, where σ is the standard deviation of the saturation drain current and μ is its mean value.

We will present the simulation method and results in detail, and how the electrical performance of the devices varies with the correlation length and standard deviation of roughness will be analyzed in the paper. In addition, the comparison between simulation and experimental results will be addressed.

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References:
1. International Technology Roadmap for Semiconductors 2005,
2. A. Asenov, S. Kaya, and A. R. Brown, IEEE Trans. Electron Devices, Intrinsic Parameter Fluctuations in Decananometer MOSFETs Introduced by Gate Line Edge Roughness, Vol. 50, 1254 (2003)
3. V. Constantoudis, G Patsis, L. Leunissen, and E. Gogolides, "Line Edge Roughness and Critical Dimension Variation : Fractal Characterization and Comparison using Model Functions", *J. Vac. Sci. Technol. B*, **22(4),** 1974, 2004.

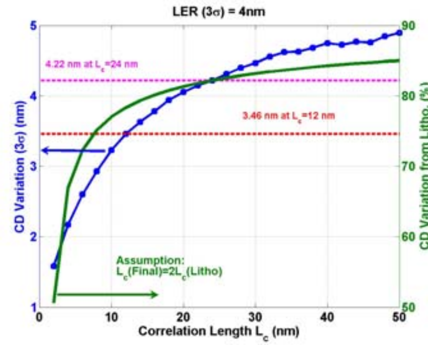
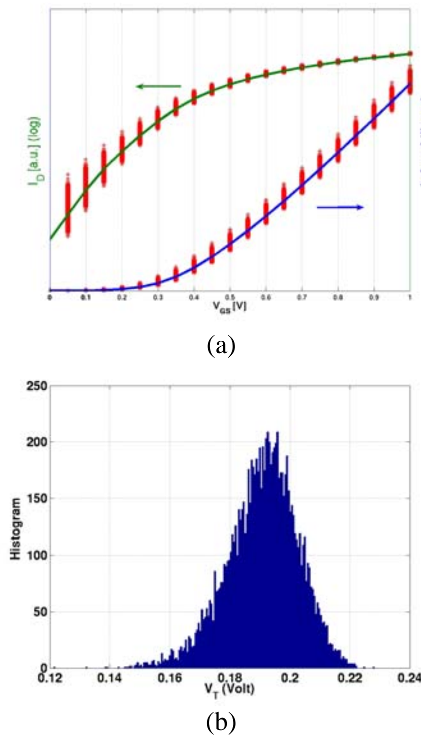


Figure 1. CD variation and the contribution of CD variation from lithography as a function of the correlation length for $LER(3\sigma) = 4nm$ and gate width = 50 nm.



(a)

(b)

Figure 2. Simulation results for (a) the drain current distributions with LER ($3\sigma_{IDsat}/\mu$=5%), solid curves are the nominal data without LER and (b) individual device threshold voltage distribution with LER (3σ=36 mV)