Focused ion beam iodine-enhanced etching of high aspect ratio holes in InP photonic crystals

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Planar photonic crystal (PhC) structures in InGaAsP/InP require cylindrical holes with a depth of 2 µm to influence the entire electromagnetic mode profile, due to the low index contrast between InGaAsP and InP. For telecommunications applications, the diameter of a hole of the PhC is in the order of 200 nm. It follows that the holes should have an aspect ratio of ~10. Until now, inductively-coupled plasma reactive ion etching (ICP-RIE) was capable of achieving such aspect ratios[1].
We show that the focused ion beam (FIB) can be used to fabricate holes with similar aspect ratios in InP, making it an accurate tool and a single step solution for rapid prototyping of PhC power splitters. We used molecular iodine under 30 keV Ga^+ irradiation and found that one of the reaction products, identified as InI_3, does not desorb spontaneously at room temperature[2]. We therefore heated the InP substrate to evaporate InI_3 and tested different temperatures to optimize: 1. etching rate, 2. surface roughness, 3. surface stoichiometry and 4. aspect ratio. All four requirements are met best at a temperature of 125 °C on the surface of the InP wafer. Etching rate was found to be 69.8 μm^3/nC, a 55-fold increase over sputtering at room temperature[2]. AFM measurement in Fig. 1 show that the RMS surface roughness increased from 0.43 nm to 10.1 nm. EDX measurements in Fig. 2 do not show I and Ga contamination, whereas the Ga-peak is clearly visible when sputtering only with Ga^+ (no I_2). In order to protect the 300 nm-thick InP cladding of the InGaAsP waveguide, 200 nm Pt was deposited by electron beam chemical vapor deposition to prevent damage and sputtering of the cladding layer by the ion beam. The Pt is removed after fabrication with very low ion fluences and XeF_2 at 125 °C. We also used ex-situ sputtered W as mask. The maximum aspect ratio obtained was 13, shown in Fig. 3. Figure 4 shows a PhC power splitter fabricated by electron beam lithography and ICP-RIE with FIB-fabricated central hole that is used as a benchmarking device to compare the fabrication quality of FIB and EBL-ICP-RIE[3].

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1 R. Wuest *et al.*, J Vac Sci Technol B **23**, 6 (2005)
2 V. Callegari *et al.*, Appl. Surf. Sci., (submitted)
3 P. M. Nellen *et al.*, Microelectron. Eng., (to be published) [accepted for publication]

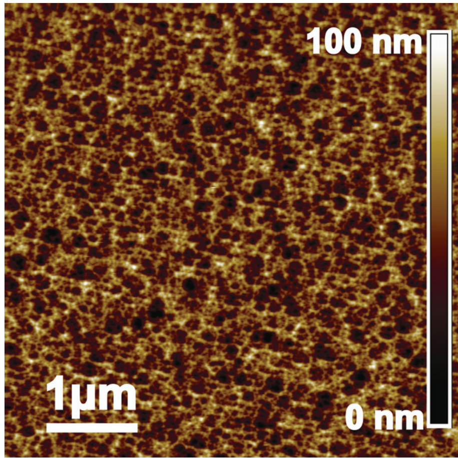

Fig. 1 AFM measurement inside a 50-µm-square etched at 125 °C. RMS surface roughness is 10.1 nm (InP wafer: 0.43 nm). Ion current was 384 pA, beam overlap -200 % and total fabrication time 29.16 s, resulting in an ion fluence of 2.84 x10^{15} cm^{-2}. The etching rate at 125 °C is 69.8 $µm^3$/nC.

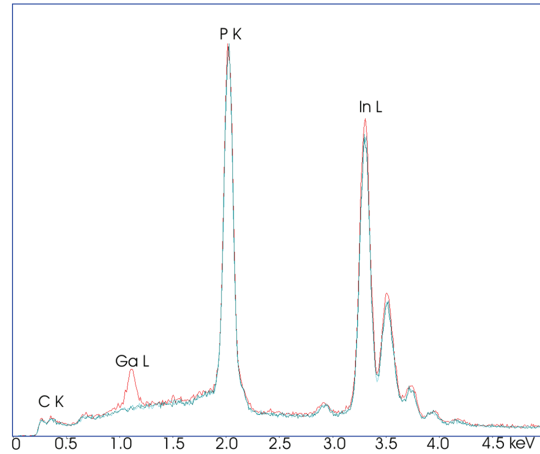

Fig. 2 EDX spectra (normalized to maximum peaks, 10 keV excitation energy) of: InP reference structure (dark blue), square etched with Ga^+ and I_2 (light blue, overlaps with InP reference) and square sputtered with Ga^+ (red, with Ga-peak). Fabrication temperature was 125 °C.

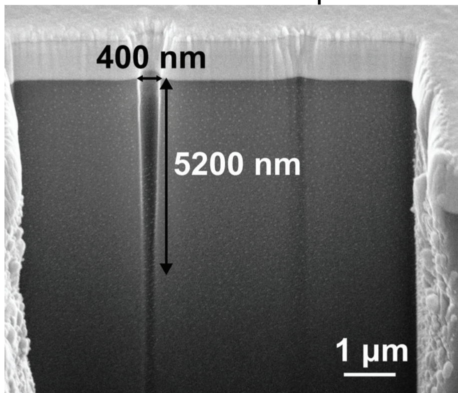

Fig. 3 Cylindrical hole etched during 15 s at 10 pA with Ga^+ and I_2 at 125 °C. Diameter of the hole at the InP surface is 400 nm. Depth is 5200 nm, resulting in an aspect ratio of 13. The 1-µm-W-protection-layer has not been removed.

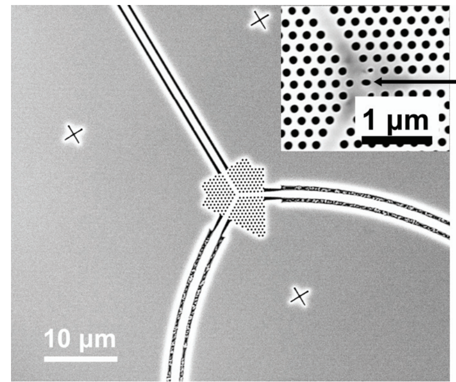

Fig. 4 PhC-power splitter fabricated by EBL-ICP-RIE before and after FIB-etching of the central hole (inset, arrow). Diameter of the central hole is 250 nm. The Pt mask has been removed with Ga^+ and XeF_2. Fabrication temperature was 125 °C, ion current 10 pA, etching time 15 s.