Development of a Hybrid Lithography Process for Fabricating Test Structures Having Dense Feature Linewidths Narrower Than 40nm

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As the linewidths of microelectronic interconnect features of high speed integrated circuits continue to decrease, the role of sidewall-surface scattering of electrons contributes increasingly to the electrical resistance of copper features, which is ordinarily limited predominantly by grain-boundary scattering. In related studies of surface and grain-boundary scattering in copper features, electrical measurements extracted from test structures usually have considerable statistical scatter, depending on the fabrication process, which is often the result of variations in the degree of sidewall scattering of transport electrons by surface micro-roughness. In this paper, we report on the development of a hybrid lithography process that combines electron-beam (EB) and optical lithography with an anisotropic wet etching process to fabricate mono-crystalline silicon test structures with sub-40-nm critical dimensions and highly controlled surface microstructures. The motivation is to provide both isolated and dense nano-scale features without having to pattern entire wafers exclusively with EB lithography, which would require long write times and delay the fabrication and generation of test results. The end applications are considered to be electron transport studies in ultra-narrow copper features having sidewall properties that are uniquely advantageous for studying surface-scattering dynamics. In addition, the hybrid lithography process appears highly useful for the fabrication of novel reference materials for scatterometry-based optical critical-dimension (OCD) and related CD-applications.

The hybrid lithography process has so far been used to fabricate electrical test structures patterned in mono-crystalline (110) silicon and having fine line features and trenches. The latter are EB defined with the contact pads of the test structures patterned by optical lithography. The fine lines and trenches are aligned in the <112> crystal direction by an orientation alignment process, with which the exact <112> crystal direction being determined using an orientation "rosette" of multiple features having slightly different orientations. After the lattice orientation of the substrate silicon is established in this manner, optical lithography is employed to pattern the large-area contact pads. Figure 1 demonstrates the hybrid test structure integration with a set of trenches aligned to contact pads after process-integration with EB lithography.

The current minimum width of the trenches that have been fabricated is approximately 100 nm, as shown in Figure 2. Development of the process to pattern trenches with sub-90nm widths to facilitate the fabrication of pure-copper features with ultra-smooth sidewalls is continuing. The minimum width of lines patterned in the substrate is less than 40 nm, as shown in Figure 3. These structures have an immediate use in CD reference-material applications.

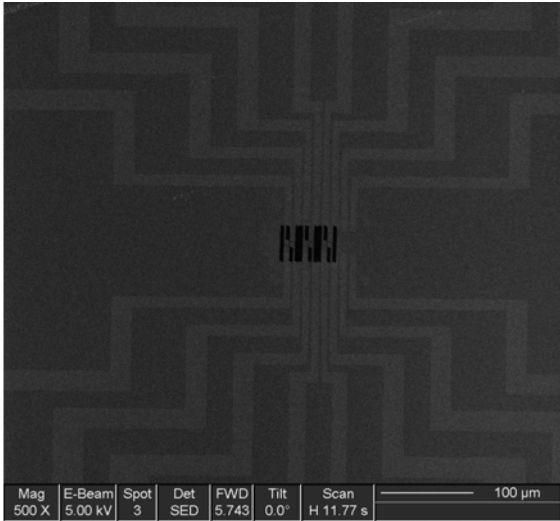

Figure 1, a set of trench structures integrated with macro-structures.

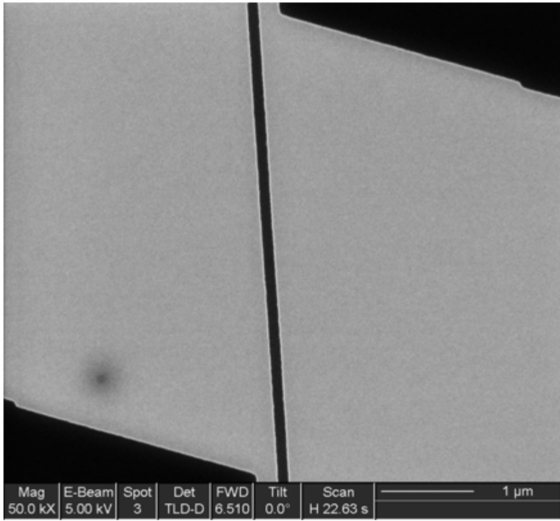

Figure 2, 100nm trench structure written using EB lithography. The trench is along the silicon <112> direction.

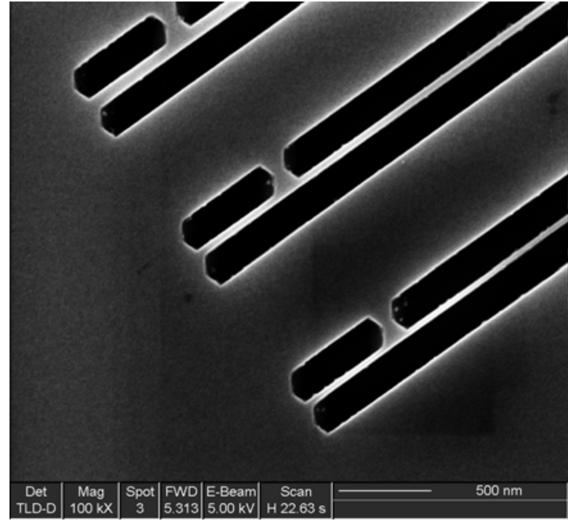

Figure 3, fine line structures. The width of the thinnest line in the figure is less than 40nm.