A novel Carbon-Nanotube-based Nano-lithography technique to form nano-MOS devices

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We report a novel submicron and nanolithography technique based on vertically aligned carbon nanotubes on silicon substrates. This technique is capable of drawing lines with nano-meter width capable of fabricating nano-scale MOSFET transistors. The growth of carbon nanotubes on silicon substrates is achieved using a plasma-enhanced CVD (PECVD) method and the seed layer for the growth of CNTs is a thin nickel layer. A vertical growth is achieved under the DC plasma power density ranges of 4.5 to 5.5W/cm^2. The higher magnification of each nanotube evidences a "tip-growth" where the nickel seed is accumulated on top of the tube (Fig.1-a).

The electron emission from the sharp nanotube tips is a well-known effect. Fig. (1-b) shows a novel encapsulating configuration which allows the formation of an electron beam emitted from the self-defined gated structure. The fabrication steps for such a gated structure require the vertical growth of CNTs, followed by CVD-deposition of an insulating film and a metallic layer deposition and patterning for current control between anode and cathode [1]. By a chemical-mechanical polishing step the buried CNT is exposed and finally an oxygen plasma ashing is needed to clean up the exposed CNT and to cause a recession in the inner CNT through burning the carbon from top to bottom. For lithography purposes, standard Shipley positive photo-resist is used as the sensitive material to electron exposure.

Since the growth of CNT's is strongly depending on the nickel seed layer, a novel refinement process is defined to start from a patterned seed layer using standard lithography as previously stated. The exposed resist-coated part is removed in its solvent and by a lift-off process one can form islands of nickel for subsequent growth of nanotubes. The resulted CNTs are now in isolated single-standing form and they can be used to draw single lines in a desired shape and place. Fig.(1-c) shows the evolution of a single-standing isolated tube from clusters of CNTs.

We have used this nano-writing approach to form the critical gate of the transistors. Once the gate is defined using nano-writing approach, the metal gate is used to define the source and drain areas. Doping is achieved by a 5nm thickness Ge/Sb alloy deposition and then annealing in 600^{o}C leading to a layer with a sheet-resistance of 500Ω/□. Gate oxide is 5nm thick, grown thermally with a measured inversion Cox of 0.7μF/cm^2 and the gate length is 100nm. Fig. (2-a) shows SEM picture of developed photoresist after nanolithography of gate and fig. (2-b) shows an un-polished cross-sectional view of the prepared transistor. Better viewing of the structure requires TEM imaging and specimen preparation is currently underway.

The current-voltage characteristics of the device are plotted in parts (a) to (c) of Fig. 3, evidencing a proper behavior. The device shows a sub-threshold slope of 100mV/decade and a threshold voltage of 50mV. Also an effective mobility of 350cm^2/V-s and a drive current of 312μA/μm are extracted for this small geometry transistor. Moreover, DIBL was measured to be 150mV/V. These results suggest that the device has a controllable short channel effect. Fig. 3(c) shows the saturation transconductance (gm) curve of the 100nm nMOS transistor with a peak "gm" equal to 2200mS/mm. Improvements of the lithography process for a "step-repeat" action as well as the fabrication of PMOS transistors and possibly small integrated circuits are being pursued.

1] Mohajerzadeh et.al. "Fabrication of novel self-defined field-emission transistors with PECVD method", presented at IEEE DRC meeting, (2004).

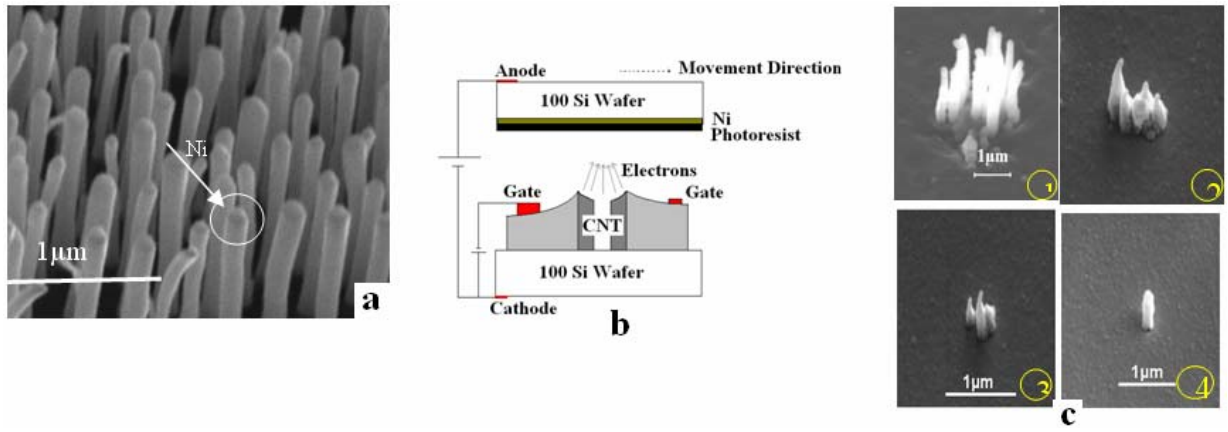

Fig 1. a) Magnified SEM image show the Ni on top of the tubes. b) Schematic picture shows nanolithography process c) SEM images of nanotubes obtained in refinement steps

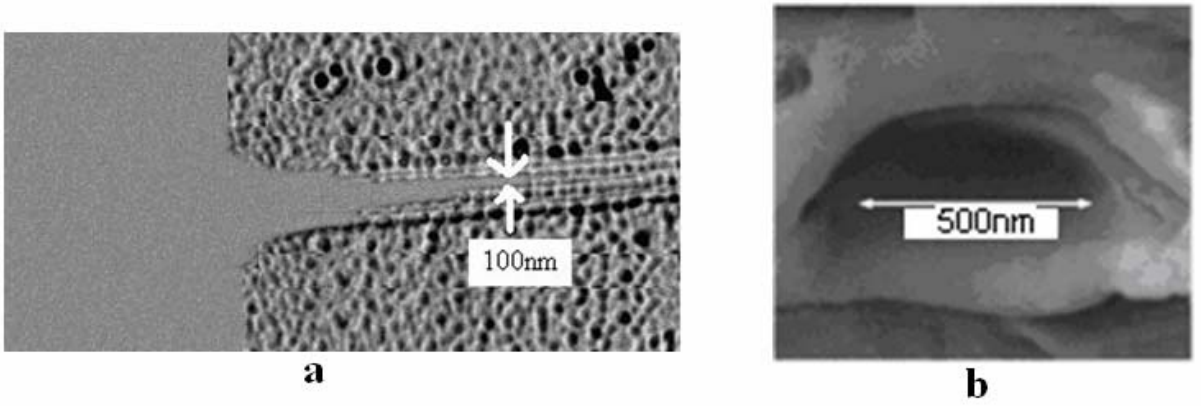

Fig. 2. a) SEM picture of developed photoresist after nanolithography of gate. b) Cross-sectional view of the prepared transistor.

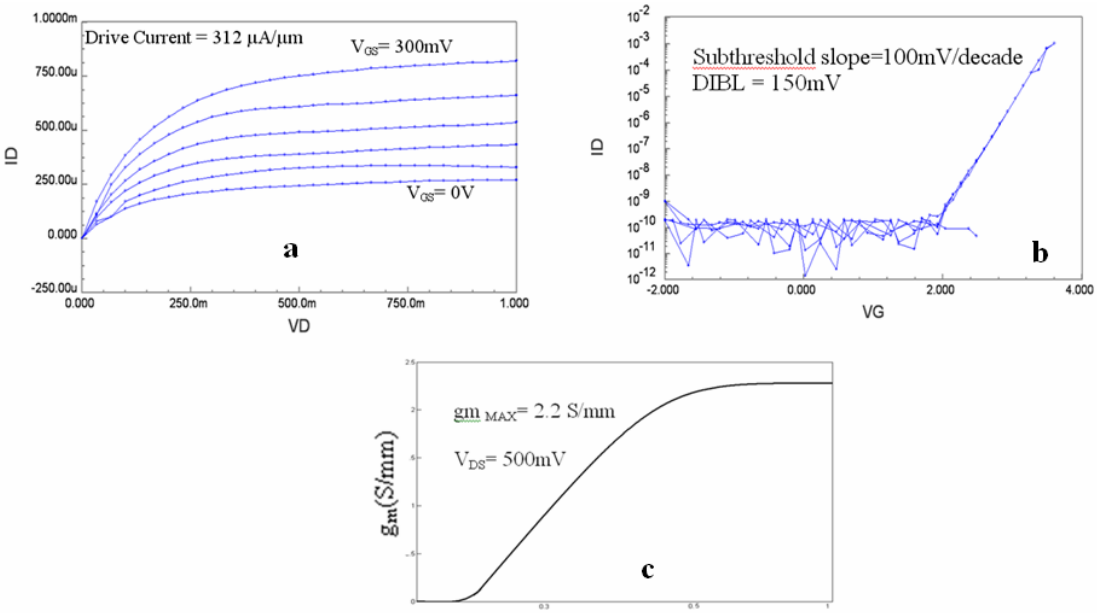

Fig. 3. a) Id-Vd family of curves for the 100nm NMOS (linear scale). b) Subthreshold Id-Vg characteristics of the nMOS transistor. c) Saturation transconductance (gm) curve of transistor