Sub-30nm hybrid lithography (ebeam/DUV) and etch process for fully depleted MOS transistors.

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The ability to perform high resolution nanostructures is fundamental to develop new microelectronic devices. The aim of hybrid lithography is to combine high lithography resolution and high throughput of optical lithography in order to decrease wafer exposure time. For that, we used Chemically Amplified Resists (CAR) which have the advantage of being fully compatible with e-beam and optical lithography with high sensitivity and resolution [1]. For this study, we used the NEB35 resist from Sumitomo Chemical.

For hybrid lithography, the main difficulty is to develop one process compatible with two types of exposure. Process should be optimized to get the best e-beam resolution and prevent standing waves generated by optical exposures [2]. E-beam exposures were achieved on a gaussian electron beam lithography equipment (Leica VB6UHR from Vistec) operating at 100 KV and DUV exposures on an ASML stepper with a wavelength of 248 nm.

For this study, amorphous carbon hard mask has been used on our structure [3]. Carbon layer offers many options for high resolution lithography because of the fact that very resist thin films (below 100nm) may be exposed. In addition, it can also be removed very easily by O_2 plasma. Therefore, carbon hard mask offers new possibilities for improving e-beam resolution. Thanks to a lower resist thickness budget to transfer into the underneath layer, ultimate resolution as well as the pattern collapse for dense lines should be improved. Finally, after plasma etching, we have succeeded in achieving 30nm MOS transistor gates (Fig. 1) and improving gate resolution down to 20nm by hard mask trimming (Fig. 2). Electrical tests onto transistor will be performed before end of January 2007.

Full 3D characterizations have also been carried out by using 3D Atomic Force Microscope (CD-AFM from VEECO) to determine the best process window. In contrast with SEM experiments, this non destructive technique allows us to have access to various parameters such as height, side-wall angles, Critical Dimension (CD), line edge roughness and line width roughness [4, 5].

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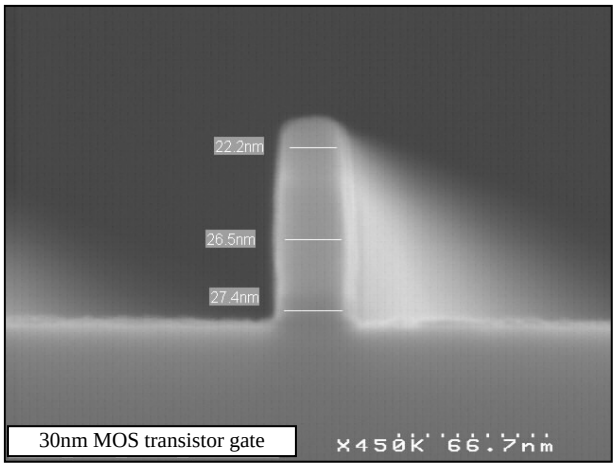

Fig. 1: SEM image of a 27nm MOS transistor gate, after etching (without hard mask trimming).

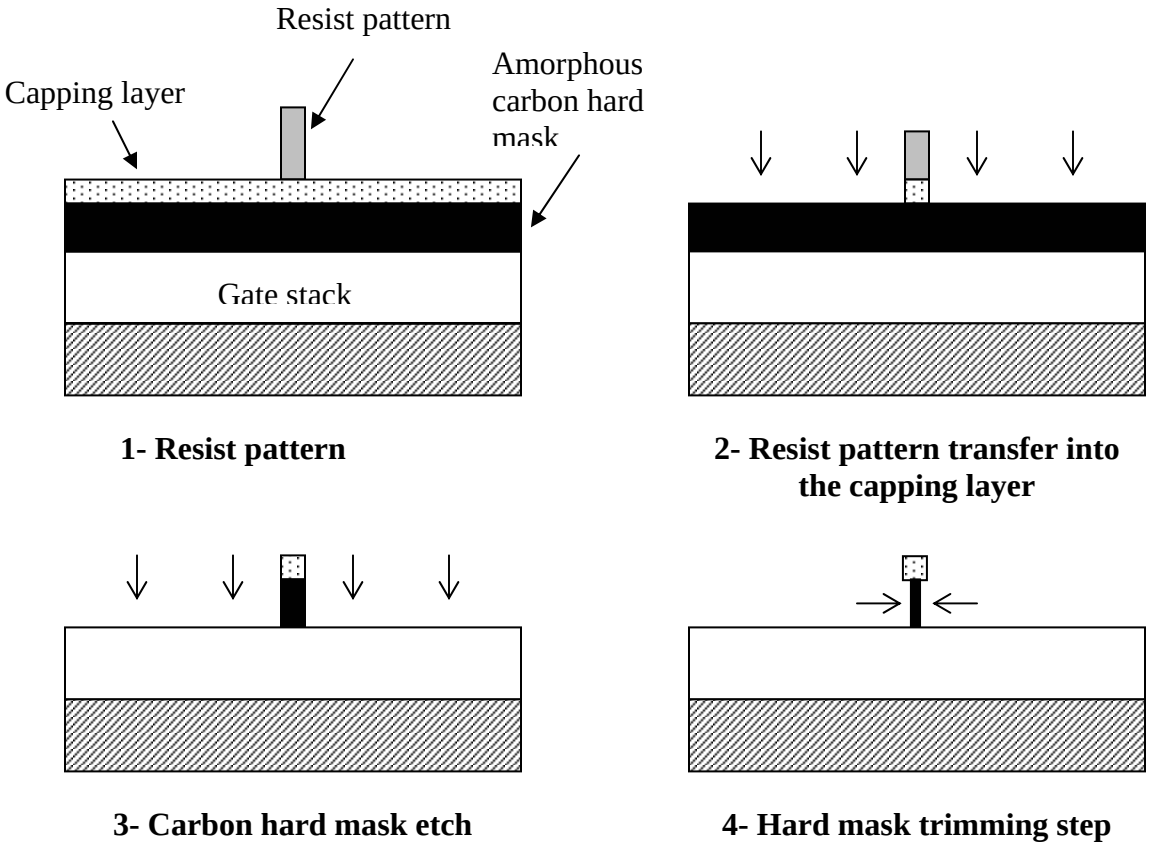

Fig. 2: Hard mask trimming process scheme