Process-induced Charging Device Damage by Low Accelerate Voltage Electron Beam Tool

Chien-Hung Lin[1], Chun-Kuang Chen[1], Tsai-Sheng Gau[1], Z.C. Wu[2], and T.I. Bao[3]

1. Exploratory Nanopatterning Technology Dept, NPTD,
2. Backend Module Dep-2, Advanced Module Technology Division,
3. Exploratory Backend Module Dept, Advanced Module Technology Division,
Taiwan Semiconductor Manufacturing Company, Ltd.
8, Li-Hsin Rd. 6, Hsinchu Science Park, Hsinchu, Taiwan 300-77, R.O.C.

Since the plasma process-induced charging damage (PID) was first reported in the 1980s[1-3], there have been many efforts to understand the phenomena, and the process effects, such as the oxide thickness, etching/ashing process, pattern dependence, bulk/SOI wafer comparison, and methodologies to monitor the charging damage. Further researches of charging damage extended from etching and ashing processes to RF sputtering, ion implantation, high-density plasma chemical vapor deposition, and electron beam curing process for low-*k* dielectrics. However, comprehensive investigation on PID caused by low accelerate voltage (<10KV) electron beam lithographic tool has not been reported in the literature. Our research results indicate that the device gate current (I_g) Wafer Acceptance Tests (WAT), shown in Figure-1, were impacted by 5KV electron beam treatment for curing low-*k* dielectric material. Further experiments with similar conditions were carried out at the metal-1/metal-2 photolithographic stages to investigate the PID issue. Monte Carlo simulation of electron penetration depth in photo-resist and low-*k* dielectric material reveals that a large number of secondary electrons would be collected by metal antenna and resulted in charging damage to device if the combination thickness of resist and dielectrics is less than 200nm. WAT results also suggest that utilize thin imaging layer on a thick electron-dissipating layer or the relatively complex tri-layer resist system can eliminate the PID.

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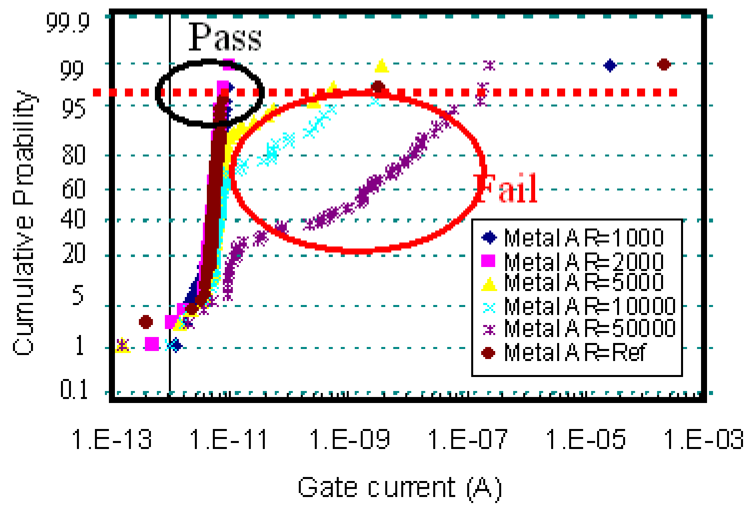

Figure 1. A WAT result shows e-beam curing process induced charging damage to the device.