Enhanced performance photonic structures using tilt-corrected electron beam lithography

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This paper shows that the performance of photonic structures can be enhanced by reducing stitch errors through the use of tilt-corrected electron beam lithography. Photonic devices are particularly sensitive to stitch errors and a number of techniques have been developed to reduce these errors. The latest generation e-beam tools have very good stitching performance (typically better than 20 nm for a VB6 UHR EWF), but this only applies to substrates which have been loaded with perfect flatness onto the stage. Any tilt gives rise to keystone field errors which result in significant stitch errors for tilts greater than 1 mrad. This can be a problem for large wafers which can bend as a result of applied film stress but it is more serious for small sections of substrate which may have to be clamped on to holders. The problem is made more severe when the substrate is already thinned as is typically the case when fabricating optical devices that need very accurate cleaving. Thinning the substrate after fabrication and just prior to cleaving has the disadvantage that any devices may be damaged. Ensuring sufficient flatness for such substrates can be time consuming, hindering throughput, or in some cases is simply impossible.

The optical structures studied here were photonic wires, 400 and 500 nm wide waveguides on a 260 nm thick Silicon on Insulator material (SOI). Because they operate in highly confined single mode regime, they allow for densely integrated silicon photonic circuits, but become very sensitive to fabrication imperfections. We deliberately introduced artificial lateral stitch errors on short lengths of waveguide to measure the effect of stitch error on the waveguide performance. Figure 1 shows both measured and simulated attenuation as a function of the lateral induced stitch error. It can be seen that for errors of 60 nm the attenuation is 0.15 dB, which is half the attenuation caused by a 1 mm length of waveguide (0.3 dB / mm propagation loss). For stitch errors of about 20 nm this reduces to a 0.015 dB loss which is negligible compared to the loss along the length of waveguide. So if long (~cm) lengths of waveguide are required it is important to keep the stitch error to about 20 nm in order to avoid significantly enhancing the losses along the waveguide.

Figure 2 shows stitch errors on a 1 μm waveguide with and without tilt correction, on a substrate which was loaded as flat as possible, but was warped because of the thinning process. The tilt varied across the substrate, but it can be seen quite clearly that for tilts up to 3 μm the tilt correction brings the stitching back below 20 nm.

In this paper we used a Vistec VB6 UHR EWF (ultra high resolution, extra wide field) tool with a 1.2 mm field. During the acceptance tests a stitch error of 13 nm maximum or 15 nm mean + 3σ was obtained on a level plate, whereas on a tilted plate (0.5 mrad) the errors increased to 38 nm maximum or 30 nm mean + 3σ. Tilt correction was performed by applying an offset to the keystone distortion of the main field during writing.

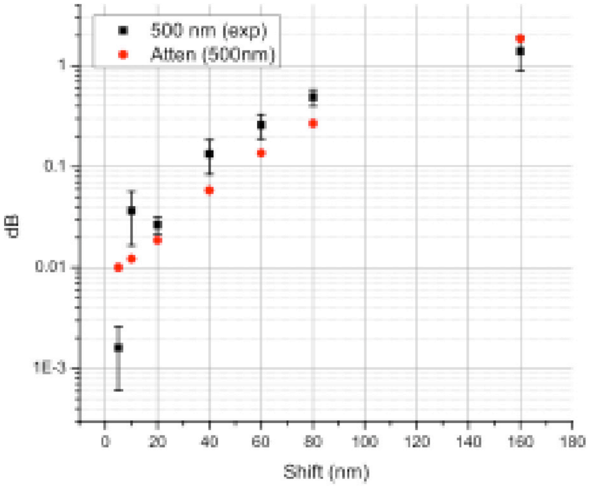
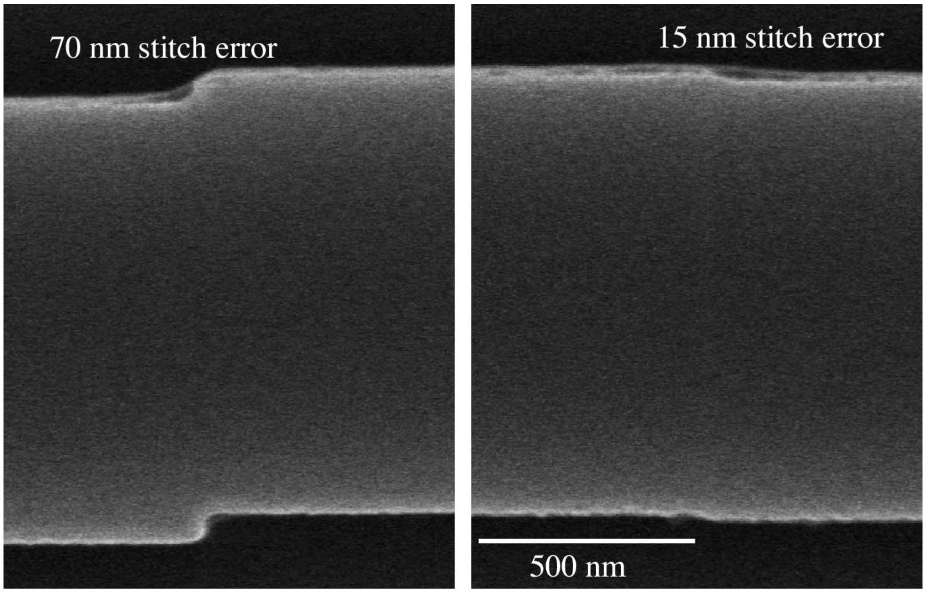


Figure 1: Measured and simulated attenuation as a function of lateral displacement error.



(a) no tilt correction

(b) with tilt correction

Figure 2: Stitch errors on a 1 μm waveguide (a) without applied tilt correction- substrate tilt was 4.2 mrad; (b) with applied tilt correction - substrate tilt was 3.0 mrad.