Location-controlled partial melt crystallization of silicon for 3-dimensional integration

D J Witte, D S Pickard, F Crnogorac, R F W Pease
Stanford University, Stanford CA 94305, USA
P Pianetta
Stanford Synchrotron Radiation Laboratory, Stanford CA 94305, USA

We report on progress toward obtaining device-quality single-crystalline regions of semiconductor on an amorphous substrate. This is desirable for monolithic 3-dimensional integration of semiconductor devices[1], where each successive circuit layer is fabricated on top of pre-existing layers. This scheme has the potential to increase circuit density, and reduce power consumption and wire delay by reducing wire lengths. There are two challenges unique to monolithic 3-dimensional integration. We must be able to obtain device-quality single-crystalline silicon on top of the amorphous spacer separating lower layers, i.e. with controllable crystallite location and size so as to avoid grain boundaries within the device channel. However, the temperature limit of the processed devices underneath must not be exceeded in order to preserve device integrity. We have previously reported results[2] suggesting that a pulsed laser crystallization process can satisfy the temperature requirement, while also allowing the formation of a partial melt in a silicon film. There is evidence that the solid lamellae inside this partial melt exhibit preferential orientation[3]; if they can be location-controlled, they may form suitable seeds for single crystals in which devices can be fabricated.

Our experimental apparatus is shown in Fig. 1; a 10W frequency doubled Nd:YAG laser beam is modulated and focused to a 25μm FWHM diameter spot. We have fabricated 200nm thick silicon films on a quartz substrate, with silicon nitride islands between 2μm and 10μm in diameter as a localized reflective layer (Fig. 2); the laser beam is aligned to the nitride islands before exposure. The resulting crystal structure (Fig. 3) for the 2μm case shows that local placement of single crystallites is possible, due to the temperature field depression caused by the reflective region (although a void has appeared at the center of the exposure). For the 10μm case, crystallization has occurred from the center outward; in the absence of a reflective island, crystallization proceeds from the edges inward. This shows the reflective region has altered the direction of crystallization, however the crystallite size is too small to achieve single crystal placement on the 10μm scale. Electron backscatter diffraction (EBSD) experiments are underway to determine whether any preferential out-of-plane orientation of the crystallites exists.

[1] J. W. Joyner et al, IEEE Trans. on VLSI Sys. **9**, 922 (2001).
[2] D J Witte et al, Microelectronics Journal **38** no 4 (April 2007), pending publication.
[3] D. K. Biegelsen, L. E. Fennell, and J. C. Zesch, Appl. Phys. Lett. **45**, 546 (1984).

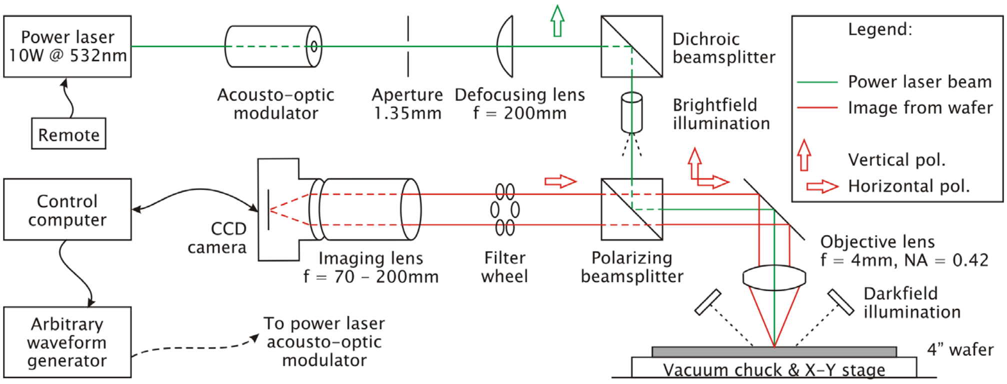


Fig. 1: Schematic of experimental apparatus.

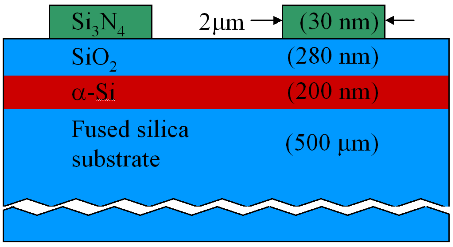
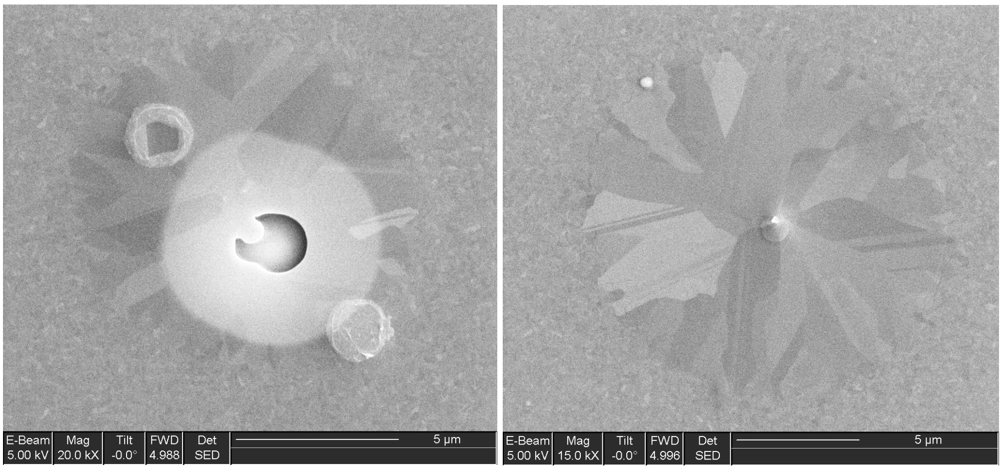


Fig. 2: Sample structure.



(a) (b)

Fig. 3: SEM images of silicon film after laser crystallization. (a) 2µm diameter 30nm thick nitride islands; 0.76W exposure for 1ms. (b) 10µm diameter 20nm thick nitride island aligned to center of beam; exposed until melting occurred.