Fabrication of amorphous metallic nanowires for IC interconnects by nanoimprint lithography

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With the line width of metal wires scales down, there is a significant increase in their resistivity due to both grain boundary and interface electron scattering. For example, the predicted Cu resistivity rise as a function of line width and aspect ratio is shown in Fig. 1 [1]. However, there have been no practical solutions to this problem to date. Since amorphous materials are lack of gain boundaries and usually have much smoother surfaces, we propose to use amorphous metals instead of ploy-crystalline ones for the IC interconnects. We also fabricated 30 nm wide amorphous metallic nanowires by nanoimprint lithography (NIL) as a demonstration.

Although pure metal thin films are usually poly-crystalline, a sputter-deposited alloy thin film could have a better amorphous-forming ability. We first chose $Al_{60}Zr_{40}$ as an example. Both transmission electron microscopy (TEM) micrographs and selected area diffraction (SAD) patterns in Fig. 3 clearly show that pure Al and pure Zr thin films are poly-crystalline while a putter-deposited $Al_{60}Zr_{40}$ film is amorphous, which is further verified by the X-Ray diffraction (XRD) data shown in Fig. 2.

To fabricate the metal nanowires, a 20 nm thick $Al_{60}Zr_{40}$ thin film was first sputter coated on a Si wafer with 300 nm thick thermal oxide. Next, a transfer layer and a UV-curable resist layer were spin-coated. Room-temperature UV-curable NIL was carried out using a quartz mold with both nanoscale features and microscale contact pads. After etching the residual cross-linked UV resist and the transfer layer, a thin layer or SiOx was deposited using e-beam evaporation, followed by a liftoff in warm acetone. Finally, chlorine based reactive ion etching (RIE) was used to transfer the pattern down to the metallic layer. The fabricated metallic nanowires are 10 μm and 70 μm long, with a width ranging from 1 μm to 30 nm (Fig. 4).

The amorphous $Al_{60}Zr_{40}$ film exhibits much lower surface roughness. Fig. 5 shows the AFM images for an Al thin film and the $Al_{60}Zr_{40}$ thin film, both on thermal oxide. The RMS roughness values for the amorphous film is 1.61 nm, much lower than that of the pure Al film (2.83 nm), suggesting that the surface roughness of poly-crystalline wires could be significantly reduced by utilizing amorphous wires.

With the removal of grain boundaries and the reduction of surface roughness in the amorphous metallic nanowire, the electron scattering effect with the size shrinking would be greatly reduced. As a result, the electrical resistivity is expected to be improved in the small feature regime. The electrical measurements, together with our exploring in other fabrication techniques and materials (e.g., Cu), will be reported too. The electrical resisitivity as a function of other parameters such as line edge roughness will also be discussed.

Reference:

1. http://www.itrs.net/Links/2005ITRS/Interconnect2005.pdf

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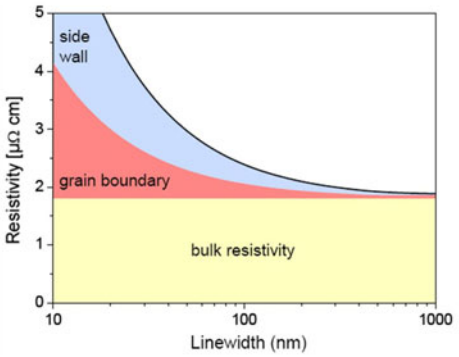

Fig. 1 Cu resistivity as a function of line width [1].

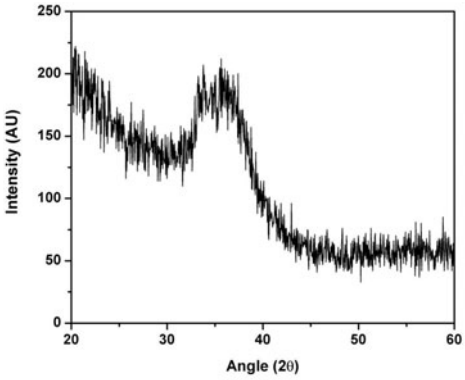

Fig. 2 XRD spectrum of the sputtered $Al_{60}Zr_{40}$ thin film.

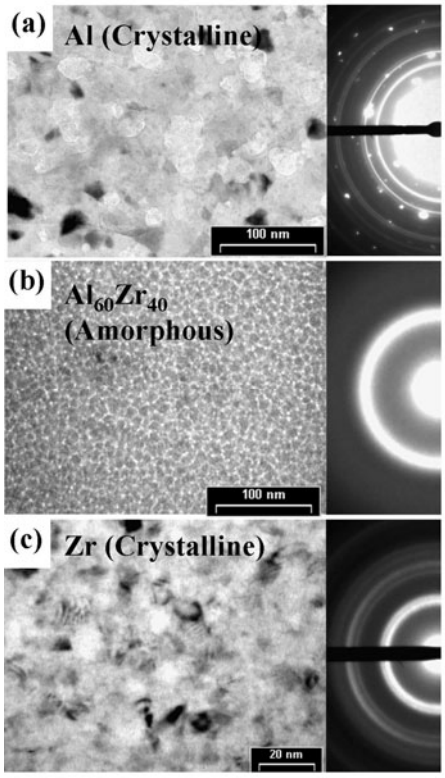

Fig. 3 TEM morphology and diffraction pattern for crystalline Al (a); amorphous alloy (b) and crystalline Zr (c).

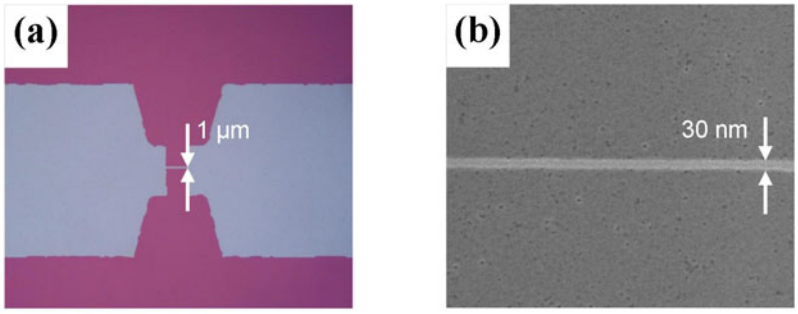

Fig. 4 (a) Optical image of a 1 μm wide $Al_{60}Zr_{40}$ wire bridging two contact pads; (b) SEM image of a 30 nm wide $Al_{60}Zr_{40}$ wire. Both are on 300 nm thick thermal oxide.

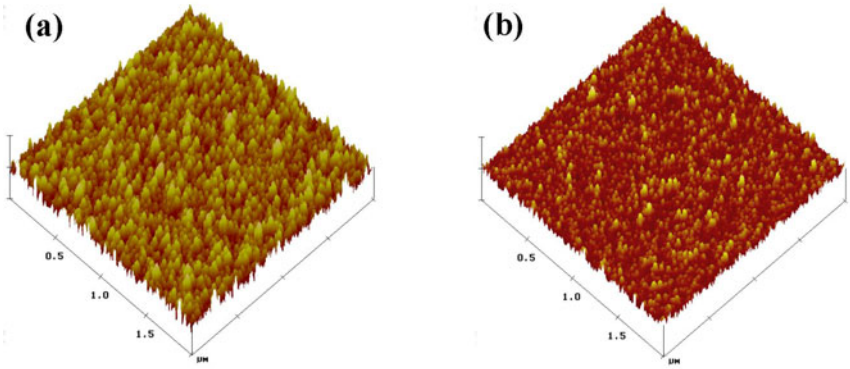

Fig. 5 AFM images of as-deposited Al (a) and $Al_{60}Zr_{40}$ film. The RMS roughness for them are 2.83 nm (a) and 1.61 nm (b), respectively.