Engineered Materials for Single Atom Architectures for Computation

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One driving force behind the microelectronics industry is the ability to pack ever more features onto a silicon chip, by continually miniaturising the individual components. However, after 2015 there is no known technological route to reduce device sizes below 10nm. In this talk we outline a complete, directed self-assembly fabrication strategy towards atomic-scale device fabrication in silicon using scanning probe lithography and high purity silicon crystal growth.

A key aspect of being able to build single atom devices is the ability to distinguish single atoms on and in the silicon surface. We demonstrate a detailed understanding of the surface chemistry to identify and control the position of individual dopant atoms using gaseous dopant sources [1]. We demonstrate that we can place individual dopant atoms in silicon at precise locations [2] and encapsulate them in epitaxial silicon with minimal diffusion and segregation of the dopants [3].

Detailed studies have confirmed the range of electrical transport characteristics that can be achieved using highly doped, planar dopants from gaseous sources [4]. We demonstrate that we can pattern this dopant layer using STM lithography and relate the electrical device characteristics at low temperatures to the presence of the lithographic patterning [5].

Using this process we have fabricated conducting nanoscale wires with widths down to ~2nm, tunnel junctions, in plane gated single electron transistors and arrays of quantum dots in silicon [6]. We will present an overview of the devices that have been made with this technology and highlight some of the challenges to achieving truly atomically precise devices in all three spatial dimensions.

[1] H.F. Wilson, O. Warschkow, N.A. Marks, S.R. Schofield, N.J. Curson, P.V. Smith, M.W. Radny, D.R. McKenzie and M.Y. Simmons, *"Phosphine dissociation on the Si(001) surface"*, Physical Review Letters **93**, 226102 (2004).

[2] S. R. Schofield, N. J. Curson, M. Y. Simmons, F. J. Ruess, T. Hallam, L. Oberbeck and R. G. Clark, "*Atomically precise placement of single dopants in silicon*", Physical Review Letters **91**, 136104 (2003).

[3] K.E.J. Goh, L. Oberbeck, M.Y. Simmons and R.G. Clark, "*Effect of encapsulation temperature on Si:P δ-doped layers*", Applied Physics Letters **85**, 4953-4955 (2004).

[4] K.E.J. Goh, L. Oberbeck, M.Y. Simmons, A.R. Hamilton and M.J. Butcher, *"Influence of doping density on electronic transport in degenerate Si : P δ-doped layers",* Phys. Rev. **B 73,** 03541 (2006).

[5] F.J. Rueß, L. Oberbeck, M.Y. Simmons, K.E.J. Goh, A.R. Hamilton, T. Hallam, N.J. Curson and R.G. Clark, *"Fabrication of quantum wires using scanning probe microscopy",* Nano Letters 4, 1969 (2004).

[6] F.J. Rueß *et al.,* Small 3, 567 (2007); Nanotechnology 18, 044023 (2007); Phys. Rev. B Rapid 85, 121303 (2007).