The Challenges of CMOS Photonics and Electronics for Enhanced Microprocessor Performance.

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The research program described in this paper intends to break the emerging performance wall in microprocessor development, arising from limited bandwidth and density of on-chip interconnects and chip-to-chip (processor-to-memory) electrical interfaces. CMOS-compatible photonic devices provide an infrastructure for deployment of a range of integrated photonic networks, which will replace state-of-the-art electrical interconnects, providing significant gains at the system level. Scaling of wavelength-division-multiplexing architectures using high-index-contrast waveguides offers one path to realizing the energy-efficiency and density requirements of high-data-rate links. Despite its indirect bandgap, Si is an excellent material for both electronics and photonics; its high index of refraction (3.4) at 1.5 μm wavelength enables significant miniaturization of waveguides, filters, couplers, detectors, modulators and other components. On a properly designed Si waveguide, over 100 wavelengths, each carrying 10Gb/s or more of information, can travel together and be selectively taken off by means of ring-resonator filters. Unifying the on-chip and I/O functions with a monolithic optical network using Si-photonics will enable the most energy-efficient balancing of on-chip and off-chip communication in future multi-core processors with large number of cores (e.g., 256 cores) and improve the system throughput up to 20x with respect to all-electrical interconnect [1].

In this presentation we describe the motivation for monolithic integration of Si-based photonic components for on-chip photonic interconnects, and describe the challenges of fabricating such photonic systems with appropriate fidelity within the constraints of a standard CMOS process.

[1] C. Batten, A. Joshi, J. Orcutt, A. Khilo, B. Moss, C. Holzwarth, M. Popovic, H. Li, H. I. Smith, J. Hoyt, F. Kaertner, R. Ram, V. Stojanovic, K. Asanovic "Building many-core processor to DRAM networks with monolithic silicon photonics"submitted to ISCA 2008.