Improvement in Line Width Roughness (LWR) by Post-Processing

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The 3σ CD variation along a segment of a line is defined as Line Width Roughness (LWR). Transistor performance can be impacted when the 3σ LWR is greater than 10% of the gate CD [1]. This is because along the gate where the CD is larger the ON current I_{ON} is reduced, and where the CD is smaller the OFF current I_{OFF} is increased. In addition, increased LWR also induces higher variance in device performance which can affect circuit stability.

So, for 22 nm node devices the maximum LWR tolerable is < 2.2 nm. The current best LWR that can be achieved in photoresists using conventional lithography is ~3-4 nm. Thus a nearly 2X improvement is needed in LWR to minimize the impact on device performance. Non-conventional photoresists such as molecular glasses [2], are expected to have lower LWR by design but are far from mature. Hence, it is expected that post-processing techniques would be needed to reduce LWR to acceptable levels.

In this paper we will investigate several different post-processing methods to reduce LWR including bakes, rinses, and various etch techniques. We will present the suitability of these methods for reduction of particular spatial frequencies and discuss the integration challenges from a manufacturability standpoint. For example (see figure on next page), we have demonstrated ~2 nm LWR after post-processing for 40 nm half-pitch (hp) features that are patterned using EUV lithography on the Intel Micro-Exposure Tool (MET)[3].

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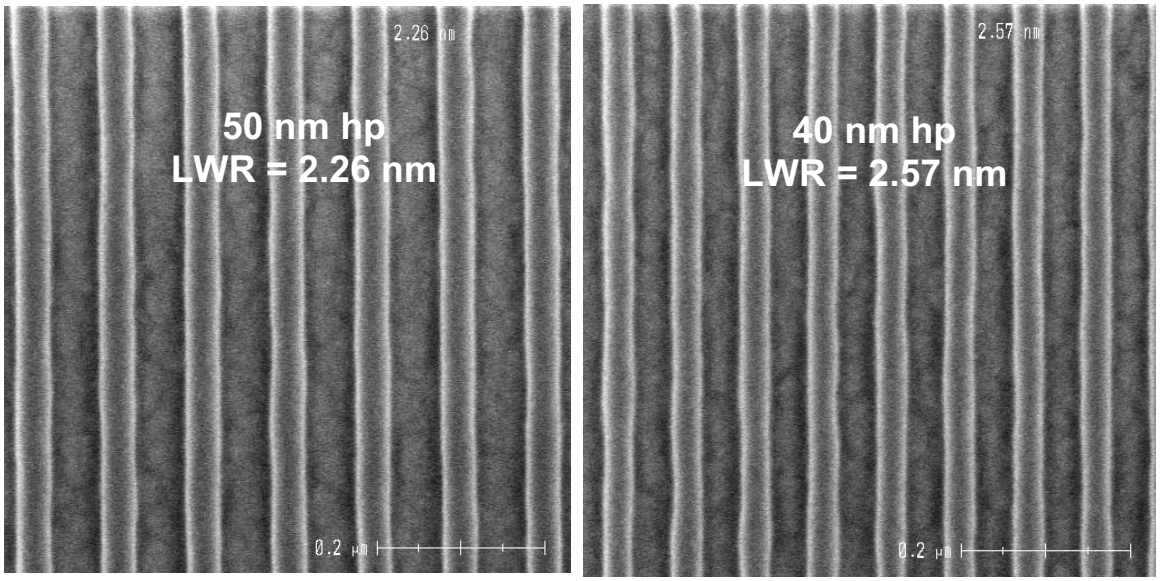

Figure 1: 50 and 40 nm half pitch (hp) resist patterns after post-processing to reduce LWR.

[1] "Impact of line-width roughness on Intel's 65-nm process devices", Manish Chandhok, Suman Datta, Daniel Lionberger, and Scott Vesecky, Proc. SPIE 6519, 65191A (2007)
[2] "Molecular glass resists for next generation lithography", Daniel Bratton, Ramakrishnan Ayothi, Nelson Felix, Heidi Cao, Hai Deng, and Christopher K. Ober, Proc. SPIE 6153, 61531D (2006)
[3] "One small step: world's first integrated EUVL process line", Jeanette M. Roberts, Terence Bacuita, Robert L. Bristol, Heidi B. Cao, Manish Chandhok, Sang H. Lee, Eric M. Panning, Melissa Shell, Guojing Zhang, and Bryan J. Rice, Proc. SPIE 5751, 64 (2005)