Full Field Imprint Masks using Variable Shape Beam Pattern Generators

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Critical to the success of imprint lithography and Step and Flash Imprint Lithography (S-FIL®) in particular is the manufacturing 1X Imprint Masks. Recently, there have been several publications addressing the fabrication of templates with 32nm and sub 32nm half pitch dimensions using high resolution Gaussian beam pattern generators. These systems are very useful for unit process development and device prototyping. In this paper, we address the progress made towards full field imprint masks suitable for the fabrication of CMOS circuits.

The starting photoplate consisted of a Cr hard mask ($\leq$ 15nm) followed by a thin imaging layer of ZEP 520A. Pattern generators such as the EBM-5000 and the EBM-6000 variable shape beam systems from NuFlare Technology were used to pattern the images on the substrates. Several key specifications of the EBM-6000, resulting in improved performance over the EBM-5000 include higher current density (70 A/cm^2), astigmatism correction in the subfields, optimized variable stage speed control, and improved data handling to increase the maximum shot count limitation.

To fabricate an imprint mask, the patterned resist serves as an etch mask for the thin Cr film. The Cr, in turn, is used as an etch block for the fused silica. A mesa is formed by etching the non-active areas using a wet buffered oxide etch (BOE) solution.

Key steps in the fabrication process include the imaging and patterning processes. ZEP520A was chosen as the e-beam resist for its ability to resolve high resolution images. This paper documents the resolution and image placement capability with the processes described above. Examples of pattern fidelity after pattern transfer into the fused silica substrate are shown in Figure 1. Half pitches down to 32nm were resolved in the imprint mask. Image placement of less than 5nm has been attained for 26mm x 32mm fields.

Finally, full field device patterns with densities consistent with what is required for circuit fabrication were written, etched and imprinted. As an example, imprinted images from the gate layer of a 38nm half pitch NAND Flash device are shown in Figure 2. The dense features are clearly resolved in both and x and y. In addition, corner features maintain their fidelity, with virtually no degradation. Linewidth roughness (LWR) is also quite reasonable, as shown in Figure 3. Depicted are the measurements on 13 lines. The critical dimension measured 39.6nm, with a LWR of only 3.7nm, 3σ. These values are comparable to the LWR obtained using high resolution Gaussian beam pattern generators.

Image placement characteristics of the imprint mask will also be presented. The prospects for further reducing the half pitch will also be discussed.

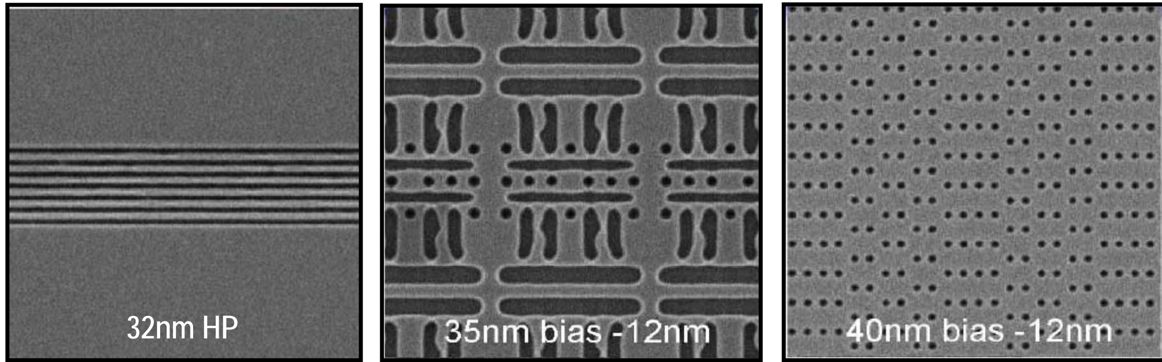


Fig 1. High resolution images from an imprint mask, patterned with an EBM-5000 VSB pattern generator, using ZEP520A as the imaging resist.

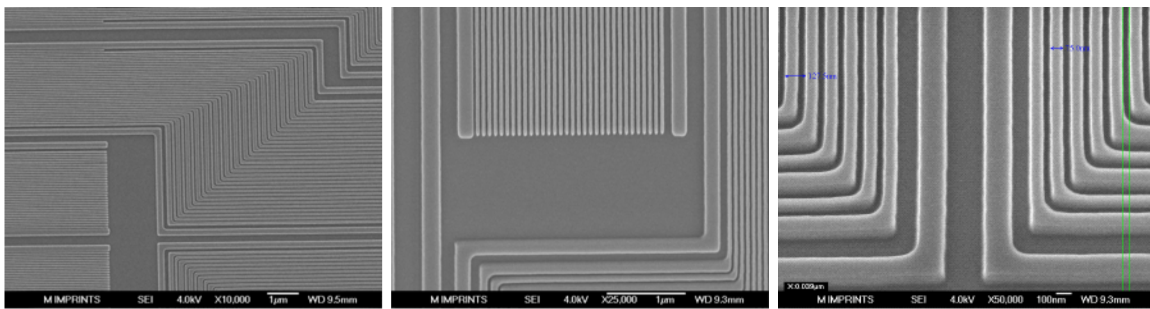
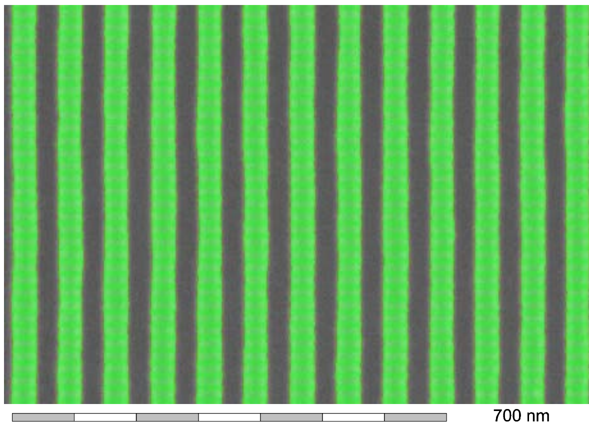


Fig 2. Imprints from the full field 38nm half pitch NAND Flash gate layer. All features are clearly resolved.



parameter	mean	standard deviation
Line Width, nm	39.575	0.646
LWR <3 σ >, nm	3.720	0.909
sigma inf <3 σ >, nm	4.291	-
Line Space, nm	34.598	1.528
Pitch Left, nm	74.231	1.741
Pitch Right, nm	74.123	1.645
Slope Angle Left, degree	95.046	0.436
Slope Angle Right, degree	94.181	0.319
LER Left <3 σ >, nm	2.883	0.758
LER Right <3 σ >, nm	2.395	0.488

Fig 3. Critical dimension uniformity and linewidth roughness across a block of 13 lines. The mean CD was 39.6nm, with a standard deviation of 0.65nm. The linewidth roughness was 3.7nm, 3σ.