Light modulation with a nano-patterned diffraction grating and MEMS pixel

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The numerous applications for MEMS-based light modulation range from communication and displays[1] to spectroscopy[2] and maskless lithography[3]. It is often desirable to have a wavelength selectable or reconfigurable aspect to such modulation. Many previous wavelength selective devices have operated on the basis of optical interference generated by reflections from multiple thin film layers. Thus, precise control of thin film layers is required; and the ability to have components side-by-side with different optical is very difficult to achieve.

We have designed, fabricated, and tested an electrostatically-actuated MEMS-based light modulator with a nanopatterned diffraction grating (Fig.1). Optical modulation in excess of 67 % is demonstrated (Fig. 2) with an electrostatic drive voltage of under 15 V and a switching speed of 0.08 ms. The nanohole pattern is designed to allow normally-incident light to couple into an in-plane grating resonance, resulting in an optical stop-band at a desired wavelength. A top fused silica plate assembled above the pixel array is used to provide a counter electrode for electrostatic actuation of the conductive metal grating. The optical properties of the modulator depend upon the proximity of the grating to the dielectric superstrate.

Fabrication of the device consists of thermal nanoimprint lithography for the nanohole grating, followed by standard microfabrication for the MEMS pixel (Fig. 4). The grating consists of an array of nanoholes patterned in either a silver or aluminum film. Shadow evaporation is used to deposit a 60 nm thick metal layer on the silicon device layer of a silicon-on-insulator (SOI) wafer, where the silicon device layer is patterned with an array of nanoholes etched 250 nm into the silicon. The silicon device layer is patterned with a plasma etch masked by a thermally imprinted layer of polymethyl methacrylate (PMMA).

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1. J. B. Sampsell, Journal of Vacuum Science & Technology B (Microelectronics and Nanometer Structures) **12**, 3242 (1994).
2. S. D. Senturia, D. R. Day, M. A. Butler, et al., Journal of Microlithography Microfabrication and Microsystems **4** (2005).
3. I. W. Jung, J. S. Wang, and O. Solgaard, IEEE Journal of Selected Topics in Quantum Electronics **13**, 147 (2007).

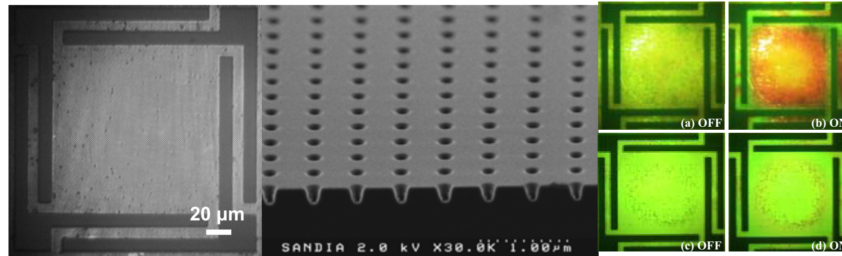

Fig. 1. (Left) Optical micrograph of MEMS pixel. The pixel is 140 µm by 140 µm square with 10 µm wide flexures. (Middle) Scanning electron micrograph (SEM) of grating pattern etched into a silicon substrate. (Right) Optical modulation from MEMS pixel with nanohole grating (a) and (b) and without nanohole grating (c) and (d). The pixels in (a) and (c) are not in contact, OFF, while in (b) and (d) are in contact, ON, with the superstrate.

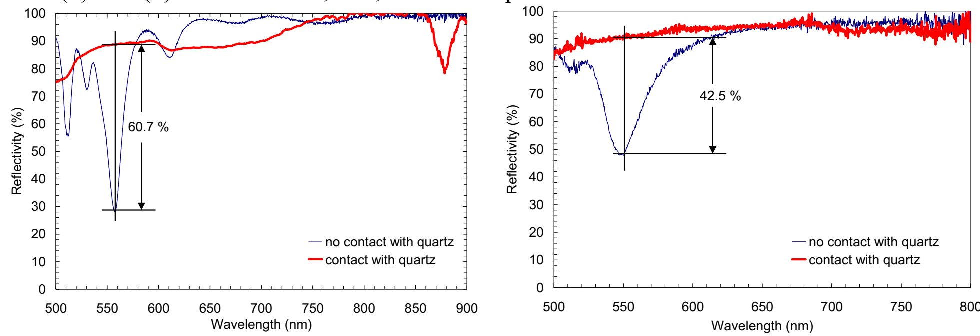

Fig. 2. Reflectivity measurements performed on large area gratings. Each grating was mounted beneath a fused silica wafer, and the reflectivity was measured with the grating pressed into contact with the glass wafer and separated by an air gap. Left: Ag grating. Right: Al grating.

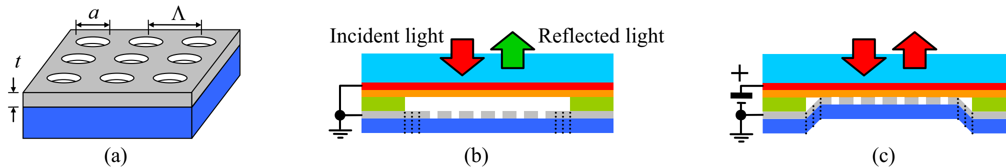

Fig. 3. (a) The pixel surface is coated with a metal of thickness *t* and patterned with a 2D square array of holes with period Λ and hole diameter *a*. (b) In the quiescent OFF state, no voltage is applied to the pixel; and an air gap separates the pixel from the fused silica superstrate. (c) The pixel is switched ON by applying a voltage between the indium tin oxide (ITO) and metal layers, causing the pixel to snap into contact with the superstrate.

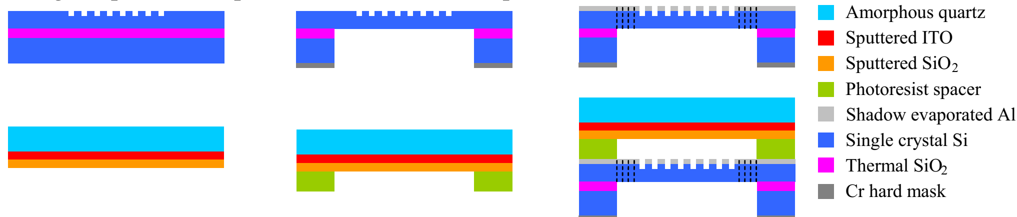

Fig. 4. Fabrication process flow for MEMS pixel. Nanoimprint lithography (NIL) was used to pattern an array of nanoholes into the Si device layer. Contact lithography was used to pattern through wafer etch holes and the MEMS pixel structure. The top plate was made by depositing ITO and SiO_2 on a quartz wafer with patterned photoresist to provide the spacing between the pixel array and the top electrode.