The Role of Computational Modeling in Semiconductor Lithography. Progressing Towards the Virtual Fab

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ABSTRACT

Computational modeling has become a core tool in the advancement of scientific and engineering fields during recent decades. It has become commonplace to use computer simulations of complex physical phenomena models to complement and often replace costly experimental work. Moreover, efficient modeling usually makes optimization feasible, and the search trajectory through parameter space that can be explored in solving optimization problems is often vastly larger than any practical experimental program could encompass. In the semiconductor manufacturing area, computational modeling and simulation have been essential in sustaining the development pace dictated by Moore's law, allowing the IC industry to maintain economic yields despite the rapidly intensifying complexity of the technology involved. In the critical area of photolithography, increasingly more accurate and extensive simulations have been employed since early efforts in the 1980's[1], including optimization of the growing number of increasingly complex resolution enhancement techniques employed to extend the capability of lithographic scanner systems. In this paper, we will review the progression of computational modeling in supporting the semiconductor industry, as well as the future trends on the use of high performance computing to accelerate development.

The foundations of today's lithographic imaging models date back to pioneering work on microscopy and diffraction in the late 19th century, including Lord Rayleigh's famous resolution equation (1879), and Abbe's classical imaging model [2], which foreshadowed both the more concrete and more compact formulation of partially coherent imaging developed by Hopkins [3], and the extension to vector imaging by Richards and Wolf [4]. Since first employed to model the lithographic process, these models have experienced continuous evolution involving reformulation for greater algorithmic efficiency, and the incorporation of a wider range of physical effects (immersion-NA vector effects, polarization, resist development and etch processes [5-13]) in order to guarantee the stringent accuracy requirements that are entailed by pushing fabrication technology to ever finer limits.

The requirement of high model accuracy on chip-sized application areas can only be met in practice by employing very sophisticated approximations of the physical phenomena involved in the lithographic exposure and development of IC wafers. This includes resorting to lengthy model calibration against empirical patterning data. Improvements in this methodology have been critical to maintaining the feasibility of full-chip simulation and correction as per-chip transistor content increases exponentially, and of course, the performance gains from each new IC generation are immediately put to work designing their successors. Nonetheless, current full-chip lithographic mask designs require hours to days of computation on clusters of a few hundred processors, in addition to the extensive period of empirical calibration.

The recent availability of very high performance computing [14] and efficient parallel algorithms offer a dramatic step forward, and in particular open the possibility of more predictive modeling of all elements of the patterning process. This will potentially enable early technology decisions prior to availability of inline tooling, acceleration of lithography development, and delivery of first-time-right patterns that hit technology goals by meeting the appropriate on-wafer tolerances at first application. Furthermore, the exploitation of deep computing and an integrated multiscale modeling and simulation flow, involving processes, devices, and technologies, is leading to a new engineering design paradigm: a full Virtual Fab for semiconductor manufacturing and nanotechnology.

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