An atom beam lithography tool for fabricating dense nanostructure arrays

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Atom beam lithography (ABL) is a proximity exposure technique where a broad beam of energetic neutral atoms floods a stencil mask and transmitted beamlets transfer the mask pattern to resist on a substrate (figure 1a).[1] It preserves the advantages of ion beam lithography including extremely large depth-of-field, sub-5 nm resist scattering, and the near absence of diffraction, yet is intrinsically free of charge-related image artifacts. Preliminary results[2] suggest a secondary electron blur of about 5 nm (σ), three times smaller than for electron beam lithography.[3] This paper reports progress toward a practical ABL technology for fabricating dense nanostructure arrays.

The approach is aperture array lithography[4] (figure 1b) where multiple offset exposures of a mask containing a periodic field of apertures is used to write the unit cells of an array in parallel. Energetic atoms are created by neutralizing an ion beam by charge transfer scattering at a crossover. The exposure tool incorporates, (figure 2a) a high brightness multi-cusp ion source and a three-electrode accelerating lens to form the crossover. We expect PMMA exposure times in the 2-10 second range, penumbral blur near 2 nm (FWHM) for a 75 µm proximity gap, and ±10% uniformity over a 6 cm field. The offset exposures will be made using a simple nanostepping concept (figure 2b) where the mask, a gap-setting spacer, and the wafer are clamped together and the entire stack mechanically inclined with respect to the beam. The rigid clamping of the mask to the substrate makes the process remarkably insensitive to vibration and thermal drift. Figure 3 shows the Morse code “CQ” written by multiple offset exposures (~30nm dia. dots). The spacing of these dots is within 0.5 nm of the design value.

The silicon masks are fabricated using the DRAM film stack in figure 4[5]. Structures written by electron beam lithography in PMMA resist are transferred to a thin sputtered SiO_2 layer by RIE and then into a thick, low stress, amorphous carbon layer with $O_2/N_2/HBr$. The carbon layer is used as a hard mask to pattern a thick SiO_2 layer using C_2F_6/C_4F_8. This SiO_2 pattern is then transferred into the silicon membrane with HBr. A backside coating of amorphous carbon protects the mask from ion implantation damage.

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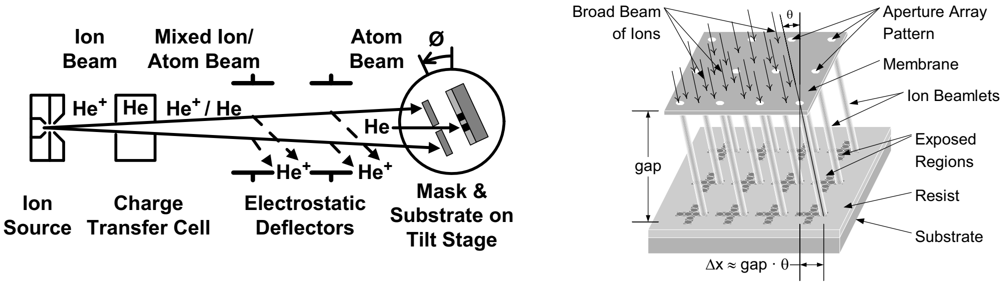
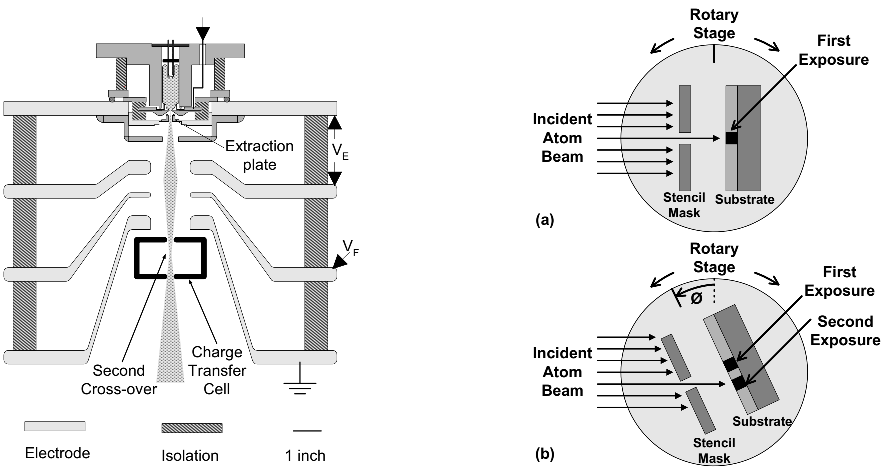
[2] Craver B, Roy A, Nounu H and Wolfe J C 2007 *J. Vac. Sci. Technol.* B **25** 2192
[3] Broers A N 1988 *IBM J. Res. Dev*. **32** 502
[4] Ruchhoeft P, Wolfe J C and Bass R 2001 *J. Vac. Sci. Technol.*B **19** 2529
[5] Mirko Vogt et. al. 2005 *Proceedings-Electrochemical Society* **2005-09** 378-387



(a) **(b)**

Figure 1. A schematic representation of (a) atom beam lithography[1] and (b) aperture array lithography[4]



(a) **(b)**

Figure 2. (a) A high brightness multi-cusp equipped He atom source and (b) the concept of nanostepping by inclining a clamped mask and substrate relative to the beam on a rotary stage[2].

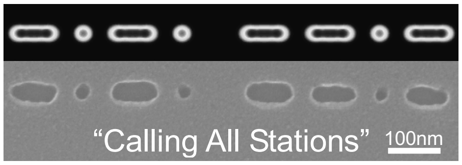


Figure 3. Morse code pattern "CQ" printed by nanostepping a single mask feature (~30 nm) 28 times demonstrates the exceptional precision and accuracy of the nanostepping process[2].

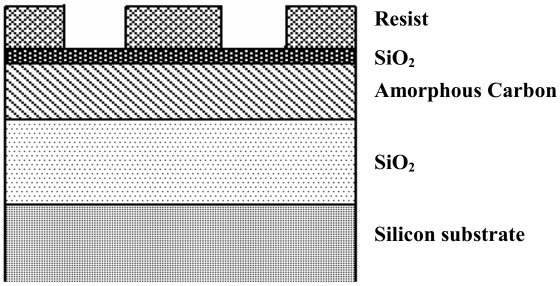


Figure 4. Schematic view of a typical hardmask stack used in DRAM processing[5].