Electron beam inspection of in-process semiconductor wafers: How, Why, and What's next?

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Since the introduction of the KLA SemSpec in the mid '90s, electron beam inspection (EBI) of wafers has grown to be a powerful tool primarily for process development and debug, but also increasingly for production defect monitoring. EBI has the unique capability of capturing subsurface electrical defects through voltage contrast (VC) that cannot be found by optical techniques. Examples including underetched contacts, NiSi pipes, and leakage from crystal defects, will be shown, along with an explanation of how the imaging technology works and how it differs from conventional SEMs.

While semiconductor technology has made tremendous strides in this time, EBI technology has only made more modest incremental improvements. A comparison between the rate of progress of EBI vs the overall semiconductor market will be drawn. Pixel counts on wafers have gone up more than 100 times, but inspection speed has not kept pace. EBI (and e-beam technology in general including SEM's and e-beam lithography) are squeezed between shot noise, resolution, and current density limits. For a simple scanning beam technology, this results in a 4^{th} order dependence of scanned area throughput relative to minimum feature size.

Strategies for dealing with the single beam throughput barrier in EBI generally have parallels in electron beam lithography. Multi-beam, multi-column, and broad-beam systems have all been under active development, although none have yet made it into commercial use. The most successful strategy to date has been to use intelligent sampling, as well as pushing the ability to detect defects that are below the resolution limit of the instruments. The ability to capture signatures of defects has proved more important than catching the defects themselves. Use of techniques to exacerbate defectivity, such as focus-exposure matrix wafers, can play an important role in the sampling strategy for process development, along with use of special test chip designs that can enhance effective throughput.