FPGA Implementation of Real-time Spatial-Phase Locking for Electron-Beam Lithography

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Scanning-electron beam lithography (SEBL) is the primary technology for rapidly generating arbitrary patterns with nanoscale features. However, SEBL's pattern placement accuracy remains poor compared to its resolution due to its open-loop nature. Spatial-phase locked electron-beam lithography (SPLEBL) has been developed to provide feedback control of electron-beam position by monitoring the signal from a fiducial grid on the substrate. Continuous, or "real-time," spatial-phase locking has been investigated for raster-[1] and vector-[2] scan Gaussian-beam systems and for shaped-beam systems.[3] Previous implementations of spatial-phase locking have used a general purpose micro-processor, a real-time operating systems, and PCI bus connected A/D and D/A converters.[1] However, this configuration limits writing speed to a few mega-pixels per second. In order to provide spatial-phase locking at the significantly higher pixel rates used by many current and emerging SEBL tools, we have implemented both raster-scan and vector-scan phase-locking algorithms on a field-programmable gate array (FPGA).

Both real-time spatial-phase locking algorithms are implemented in a Vertex IV FPGA in Xilinx's XtremeDSP Development Kit-IV. A 14-bit ADC samples the grid signal at up to 100 mega-pixels per second, and two 14-bit DACs provide output for the x- and y- position error corrections. Fig. 1 shows a diagram of the FPGA design including both custom and Xilinx-based blocks. FPGA design model simulations are shown in Fig. 2. These simulations indicate that the beam position can be estimated with nanometer precision by the FPGA after sampling relatively few pixels. The slight slope observed in x-position error and the residual y-position error can be potentially eliminated by applying an appropriate window function to the time sequenced data. In addition, the relatively low cost and compact implementation of the FPGA design allows straightforward parallelization of the system for multiple electron beam systems.

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2 Y. Yang and J. T. Hastings, J. of Vac. Sci. Tech. B. **25**, 2072 (2007).
3 J. G. Hartley, T. R. Groves, H. I. Smith, et al., Rev. Sci. Instrum. **74**, 1377 (2003).

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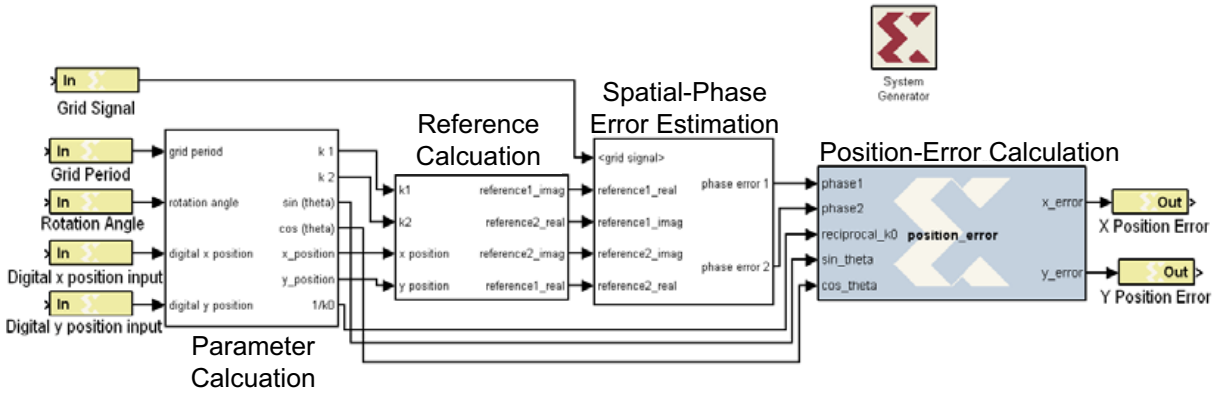

Fig. 1 FPGA design model built in Simulink for real-time spatial-phase locking. Parameter calculation, reference calculation, and spatial phase error estimation are subsystems built using both custom and Xilinx-based blocks.

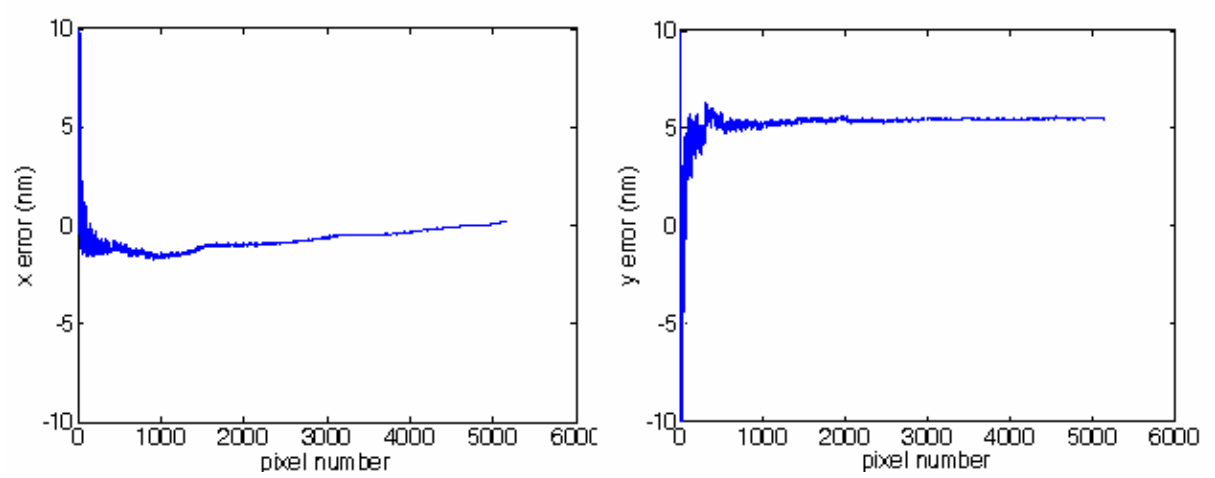

Fig. 2 Estimated x- and y- beam position errors as a function of number of sampled pixels from FPGA design model simulation. (Grid period: 200nm, sample spacing: 41.2nm, rotation angle: 20°, signal-to-noise-ratio: 1×10^{9}, 100x50 pixel feature, flyback fill strategy)