Self-Assembly of Individual Vertically Aligned Carbon Nanotubes

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Nanoscale electronic devices made from carbon nanotubes such as transistors[1] and sensors[2] have shown great results, however, challenges in integrating nanotubes at precise locations with predictable properties have thwarted their use in wafer scale fabrication. Conventional microelectronic devices consist of many metal levels[3] which are not stable under high temperature CVD processing that is used to grow CNTs.[4] In this study, we present a novel fabrication technique, at room temperature, for self-assembly of vertically aligned single walled carbon nanotubes which can be used as transistors, interconnects or biosensing probes. The deposition of single high-aspect-ratio particles such as carbon nanotubes may be done at the center of sub-100 nm windows in insulating thin films over metal using electrophoresis. A nanoscopic lens is formed when higher mobility ions in a suspension containing the particles charge the surface of the insulator and modify the electric field that draws the particles towards the metal at the base of the window. Once a single nanotube is deposited and makes electrical contact with the metal, under certain conditions, no more nanotubes will be deposited at the base of the window because of the electric field around the deposited nanotube. By changing the geometry of the window accurate control of the number and spacing of deposited nanotubes can be achieved. Observations are supported by the field emission scanning electron microscope images, micro-Raman spectroscopy and finite element analysis. This method provides a large degree of control over the deposition, firstly, by varying the solution consisting of purified semiconducting or metallic nanotubes and, secondly, by varying electric field and geometry of windows. Devices such as vertical field effect transistors and interconnected nanoprobe arrays may now be fabricated in the metal levels of CMOS integrated circuits (using current generation optical lithographic tools) to facilitate three-dimensional polylithic circuit architectures.

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