Low Temperature limits for Nano-Graphoepitaxy of Semiconductors

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Key words: graphoepitaxy, crystallization, nanoimprint, heat flow

Early investigations of graphoepitaxy have shown that surface relief grating structures of 3-5μm pitch in amorphous substrates can define the crystallographic orientation of deposited silicon films[1]. The melting and recrystallization of these thin films has been performed using strip-heater ovens as well as by high power continuous wave (cw) lasers. In both of these methods, the substrate was temperature biased to a large fraction of the melting temperature allowing for a slow cooling rate, yielding large single crystal grains over 10μm in size.

The authors identified an opportunity to use such a process to control the orientation of device quality semiconductor islands on amorphous substrates as an upper layer of a three dimensional integrated circuit (3DIC) [2]. However, to avoid damage to the underlying device layers of a 3DIC during recrystallization, low temperature techniques such as laser transient heating were employed (pulsed frequency doubled Nd:YAG laser). In addition, a much smaller grating of 190nm pitch was fabricated in SiO_2 using nanoimprint lithography (NIL) in order to impart better orientation control.

Early experiments[3] indicated that we needed slower cooling of the crystallizing liquid semiconductor to allow larger single crystal domains (grains) with low defect density and a sharper template pattern.

Here we report on experiments addressing both issues. Current investigation uses a template of inverted pyramids (500nm) fabricated by orientation dependent etching (30% KOH at 80ºC) to produce atomically sharp geometries. The crystalline substrate is masked by 12nm of thermally grown SiO_2 over which an amorphous silicon layer is deposited by LPCVD (60nm, 525ºC). The structure is capped with 1.2μm of low temperature oxide (LTO, 400ºC) and annealed using a single 100μs pulse of Nd:YAG laser (λ=532nm). The long pulse duration not only melts the α-Si film, but also artificially temperature biases the silicon substrate reducing the cooling rate. The resulting crystal grains are 200-400nm in size and seem to have agglomerated, lifting the LTO cap (Fig.1). The HRTEM images illustrate high crystalline quality and grain orientation matching that of the silicon substrate (Fig.2).

We conclude that due to geometry and heat flow considerations, there is a trade-off between the size and quality of recrystallized grains and the low substrate temperatures required for 3DIC fabrication.

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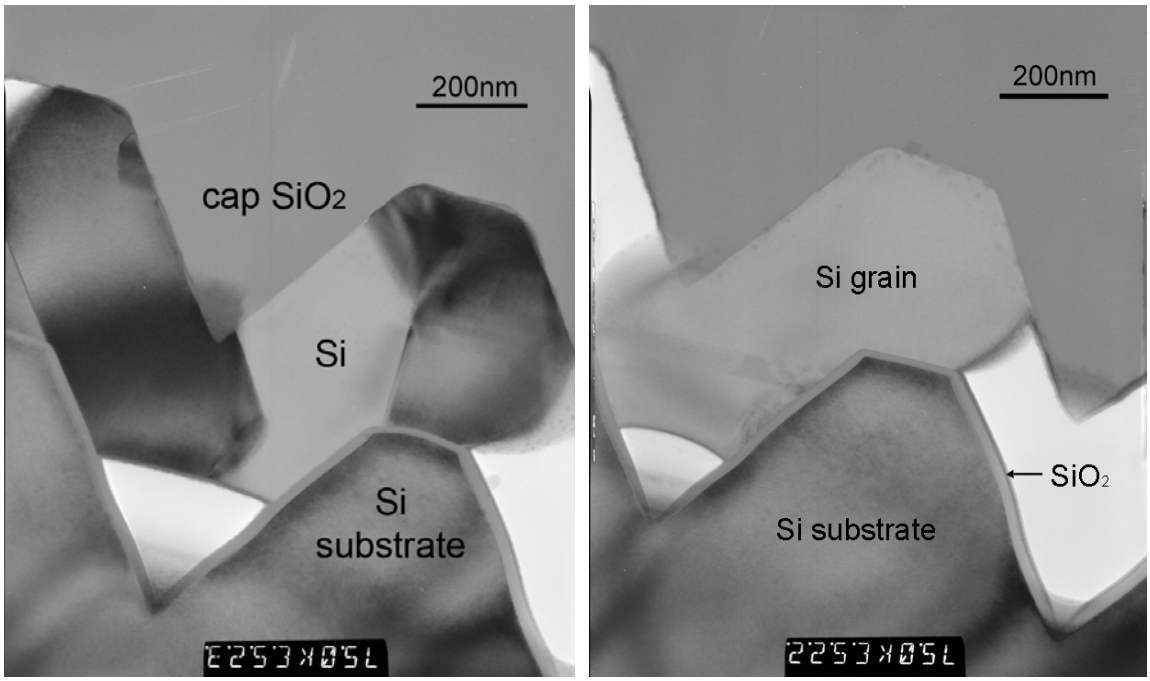

Figure 1. TEM cross-section of the laser annealed structure. The light gray material covering the Si substrate is 12nm of thermal SiO_2.

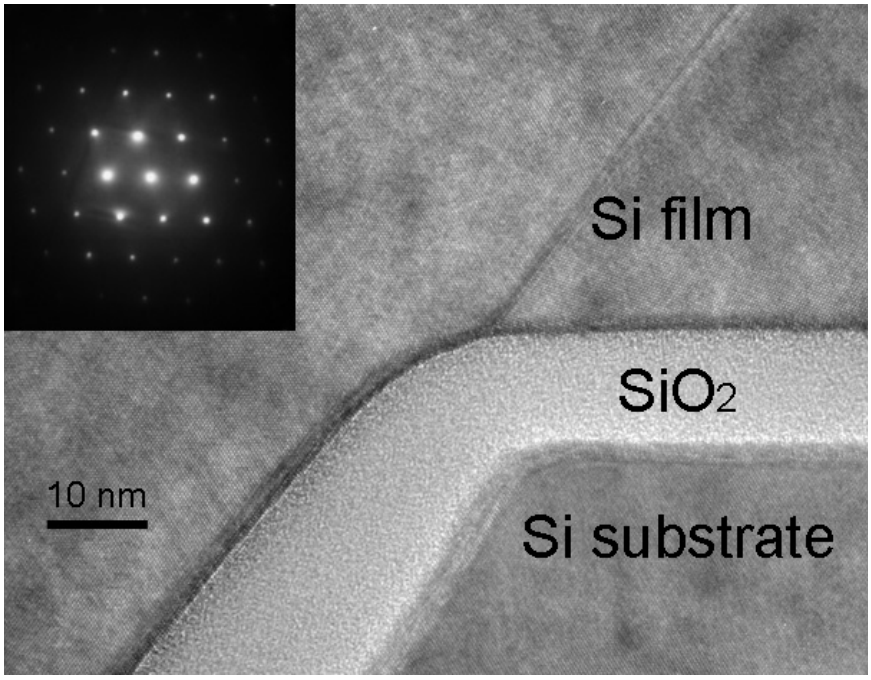

Figure 2. HRTEM cross-section of the recrystallized film showing high quality crystal grain with a single stacking fault. Inset: micro diffraction (CBED) pattern of the grain.

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