Graphene Transistors Fabricated via Transfer-Printing in Device Active-Areas on Large Wafer

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Graphene is of great interests as an emerging electronic material because of its exceptional semiconducting properties, such as high carrier mobility (up to 20,000 cm^2/Vs), high carrier concentration, a stable 2D thin crystal structure, and potential to enable ballistic transport at room temperature [1].

However, presently high-quality graphene sheet is only available in small area of 100s μm^2, and not yet available over large wafers which are needed for mass production. In this paper, we report and demonstrate a novel method to precisely print exfoliated high-quality graphene sheets in the device active-areas over entire wafer, thus overcoming the current difficulties in getting large graphene wafers. And we report the fabrication of high performance graphene transistors on the printed graphene [2].

In our method, termed "graphene-on-demand by cut-and-choose, transfer-printing (DCT)" (Fig.1), a DCT stamp of pillars is pressed into a graphite substrate to cut and exfoliate a graphene sheet. Then an inspection of graphene quality decides if the graphene sheet will be printed onto the device active-area on another wafer. The DCT process can be repeated to place graphenes on all device active-areas of an entire wafer. The alignment marks on the stamp and wafer assure a high precision placement of each graphene patch in a device active area. In DCT, the adhesions of graphene with the stamp and the printed substrate are controlled to ensure exfoliation and transfer-printing.

Fig. 2 shows the scanning electron micrographs (SEMs) of (a) a DCT stamp bearing 15 μm diameter pillar array, and (b) the array of graphene patches cut and printed by the stamp shown in (a). The shape of graphene cuts is almost the same as the pillars on the stamp, indicating that most of the cut was caused by high-shear-stress-induced fractures at the stamp edges, not by tearing, and hence assuring a high-fidelity cutting. The graphene cuts as small as 1.5 μm were also printed by using this method.

We have fabricated field-effect transistors (FETs) on the graphene printed on a SiO_2 surface thermally grown on a p^+ Si substrate, which serves as a back-gate (Fig. 3 (a)). Thickness of graphene channels ranges from 1.2 nm (~ 4 monolayers) to 3 nm (~ 9 monolayers). Fig. 3 (b) plots the I_{DS}-V_{GS} characteristics of a FET with the graphene thickness of d ~ 1.5 nm, and shows that the gate can induce either hole or electron conduction (i.e. ambipolar behavior). The hole and electron mobilities were extracted to be μ_h = 3,735 cm^2/Vs and μ_e = 795 cm^2/Vs, respectively, and the maximum drive current (I_{DS} / W) at V_{DS} = 1 V is 1.7 mA/μm. The mobilities and the drive current are among the highest values reported.

In summary, we report a method, in which a well-defined stamp is used to precisely cut, exfoliate, and transfer-print graphenes into device active-areas. The method has been experimentally demonstrated by making working FETs with good transport properties. Such approach might be applied to fabricate graphene integrated circuits on large wafer.

[1] Geim; A. K. and Novoselov; K. S. Nature Materials **6**, 183-191, (2007)
[2] Liang; X.G., Fu; Z.L., Chou; S.Y. Nano Lett. **7**(12), 3774-3780 (2007)

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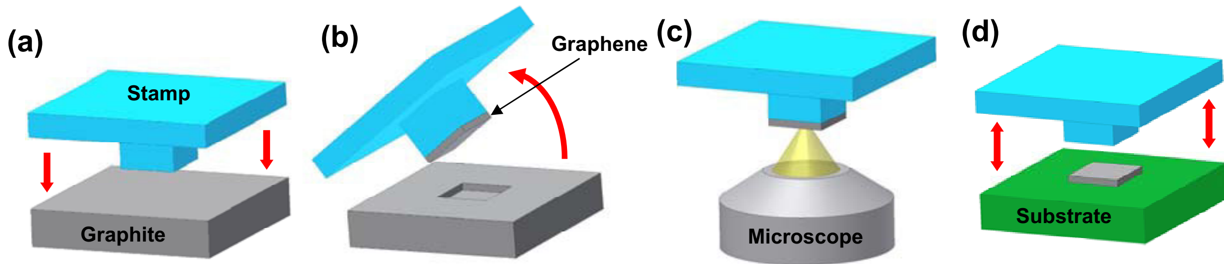

Fig. 1. Schematic of graphene-on-demand by cut-and-choose transfer-printing (DCT). (a) Press the DCT stamp into a graphite substrate; (b) the stamp cuts the graphite surface using its protrusion edge, and then the separation of the stamp from the graphite exfoliates the cut graphene sheet; (c) Inspect the quality of graphene attached on the stamp protrusion; and (d) transfer the graphene sheet onto the device active-area of another substrate.

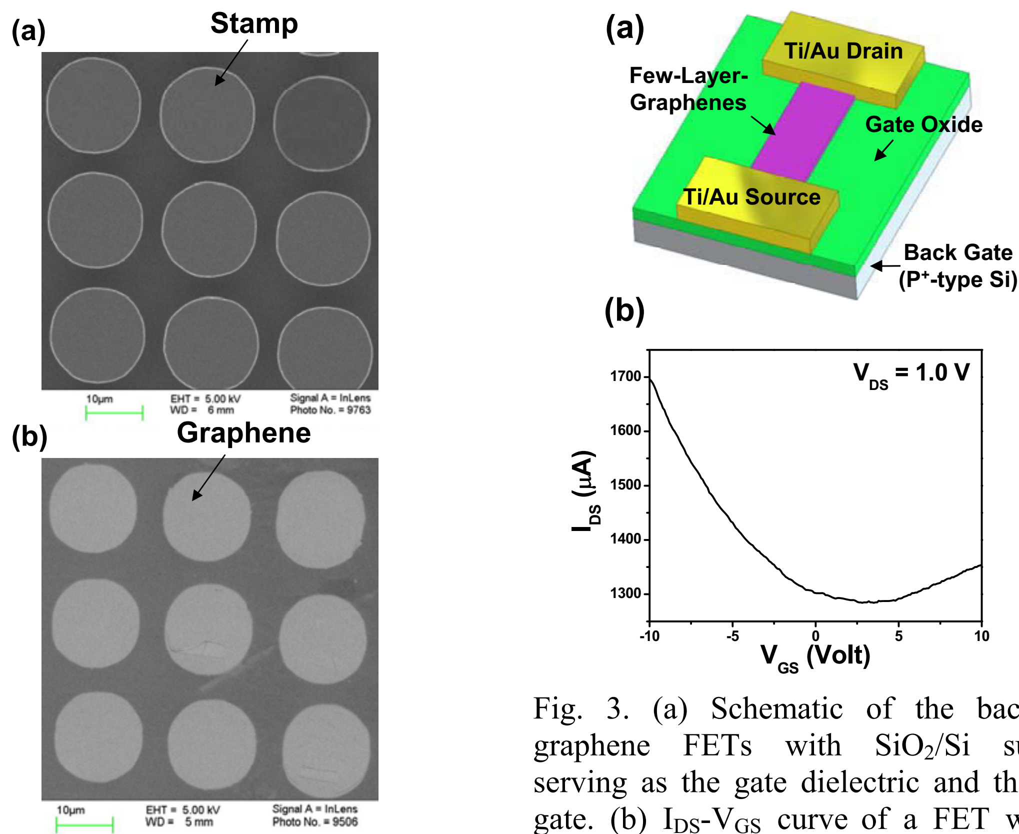

Fig. 2. SEMs of (a) a DCT stamp bearing 15 μm diameter pillar array, and (b) the graphene flake array that was cut from a graphite and transfer-printed on a SiO_2 surface of another substrate using the DCT stamp shown in (a).

Fig. 3. (a) Schematic of the back-gated graphene FETs with SiO_2/Si substrate serving as the gate dielectric and the back-gate. (b) I_{DS}-V_{GS} curve of a FET with the graphene thickness of d ~ 1.5 nm; the gate oxide thickness of t_{ox} = 20 nm; the graphene channel width of W = 1 μm; the channel length of L = 10 μm. The hole and electron mobilities were extracted to be μ_h = 3,735 cm^2/Vs and μ_e = 795 cm^2/Vs, respectively, and the maximum drive current (I_{DS} / W) at V_{DS} = 1 V is 1.7 mA/μm.