Design and Fabrication of Vertical Nanowire Device Arrays

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We report a method of fabricating vertical nanowire (NW) two terminal device arrays with high spatial registry that exploits electron beam lithography and electrophoretic assembly of the NW growth seeds. Interest in applications of semiconducting nanowires (NWs) for device and sensing purposes has grown rapidly in recent years due to their high quality and promising electronic properties. Currently, the majority of NW devices are fabricated in-plane (2-D) by removing the nanowires from the native growth substrate, dispersing them on suitable substrates, and applying electrodes. Here we report on a directed assembly approach to fabricating NW devices (Fig. 1), taking advantage of their inherent out-of-plane growth orientation. Highly doped Si (111) substrates are used for vertical, epitaxial NW growth and as well as to provide electrode back contacts for electrical characterization. Previously, one of the main limitations in fabricating vertical NW device array architectures has been in obtaining the spatial registry of the NW positions. We report a method of defining Au seeds with high spatial registry using electron beam lithography (EBL) followed by electrophoretic assembly of gold colloids (Fig. 2). Electrically doped vertical NWs (Fig. 3) are then grown by the vapor-liquid-solid (VLS) method in a cold-wall chemical vapor deposition system. The growth and characteristics of Si NW can be tailored by controlling the flow of silane precursor gas along with physical parameters (e.g., temperature and pressure) inside the growth chamber. The structure of NWs is reinforced with stand-off structures and sacrificial filler layer. The dielectric filler layer can be dissolved to expose the length of the NWs for the purpose of sensing applications. Intermediate steps of chemical mechanical polishing, oxygen plasma etching etc, are performed to planarize the device and expose the tips of NWs. Top metallic contacts are then deposited to realize two-terminal out-of-plane NW device arrays. We will report on the challenges encountered in assembling the devices and addressing individual elements within a device array, as well as discuss results of preliminary electrical characterization of the NW devices.

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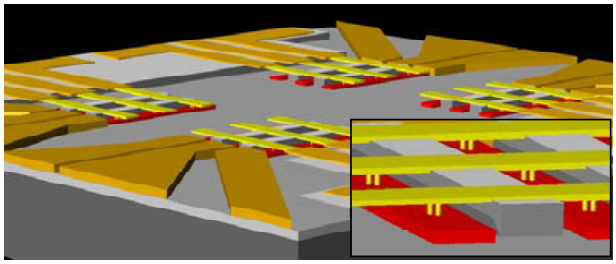

Figure 1: Schematic diagram of the out-of-plane NW device architecture. Inset: Schematic diagram of NW sandwiched between electrodes

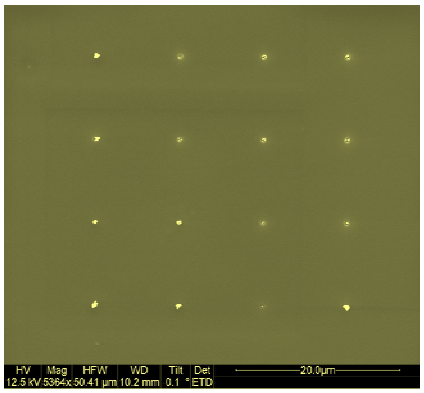

Figure 2: SEM image illustrating colloidal Au seeds in EBL patterned arrays by electrophoretic assembly.

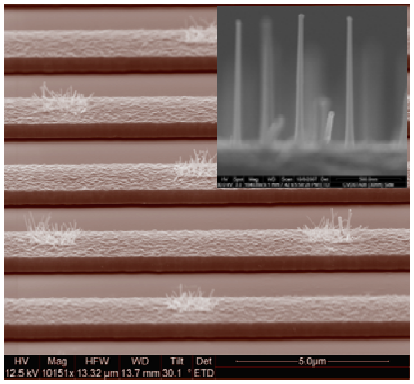

Figure 1: SEM image of NWs grown on EBL patterns. Inset: SEM image of individual NWs.