A Novel Method for Fabricating Sub-16 nm Footprint T-Gate Nanoimprint Molds

Can Peng, Xiaogan Liang and Stephen Y. Chou
Nanostructure Laboratory, Department of Electrical Engineering
Princeton University, Princeton, NJ 08544, USA

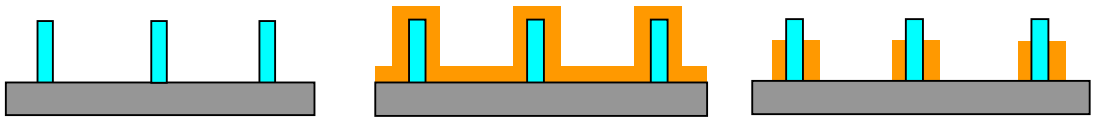
A key to improve RF transistor speed performance is to shrink the footprint of T-gates well below 100 nm [1]. This poses serious challenges to current T-gate fabrication, which uses e-beam lithography with hetero-resist stack [2, 3]. An attractive alternative method is use nanoimprint lithography (NIL). But NIL needs an effective method to make a mold. Here we report and demonstrate a novel approach to fabricate 16 nm footprint T-gate. The footprint is significantly shorter than previously reported. The novel approach offers two advantages: the T-gate footprint can be substantially smaller than an original one made by EBL, and the footprint and the T-top of the gate can be easily self-aligned during the mold fabrication.

The novel mold fabrication method has three key steps: (a) use EBL (or other lithography) to create a "scaffold" mold, which has only T-gate footprint patterns but not the T-top; (b) use etching to reduce the width of the footprint patterns on the scaffold-mold; and (c) use the modified scaffold-mold, nanoimprint, conformal deposition, and edge patterning to construct the final mold (termed "composition" mold) that has complete T-gate structure with both footprint and T-top part.

The details of the T-gate mold fabrication is shown in Fig.1. First a scaffold-mold was fabricated that has SiO2 grating of 90 nm width on a Si wafer. Each grating figure will serve a scaffold to build T-gate on the final-mold. Then the linewidth of the SiO2 grating on the scaffold-mold was shrunk to sub-20 nm in a well-controlled etching in HF or BOE solution. The scaffold-mold was used to create the final mold by making the footprint lines first on the final mold substrate, followed by self-aligned edge definition of the rest of the T-shape. In the edge definition, a 15 nm thick layer of SiNx by LPCVD was deposited on the footprint lines, and the sample is etched by RIE. Due to the etching selectivity between the SiNx layer and the SiO2 cores, a T-gate shape mold is formed.

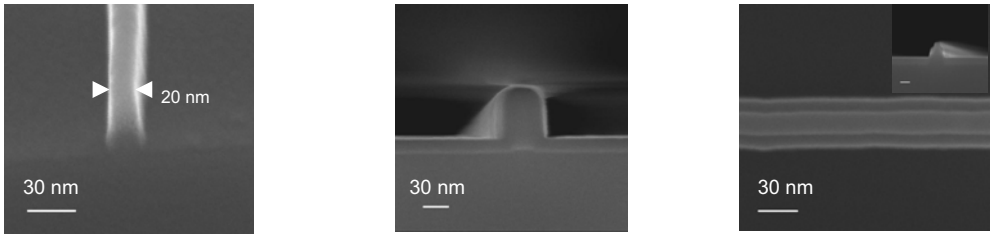
Fig. 2 shows the fabricated T-gate molds with 16 nm foot width, which is to our knowledge the smallest reported. Then the mold is thermally imprinted into resist. After removal of the residual layer by RIE, a metal deposition and lift-off created a T-gate (Fig. 3). Clearly, the method can be scaled up to wafer size mold. The large area together with the high resolution that exceeds EBL, easy self-alignment and simple fabrication steps, the method offers an effective low cost way to create sub-20 nm T-gate molds for high-performance RF circuits.

[1] D. A. Moran, H. McLelland, K. Elgaid, and et. al., *IEEE Trans. Electron. Devices,* Vol 53(12), 2006.
[2] M.T. Li, L. Chen, and S. Y. Chou, *Appl. Phys. Lett.,* Vol 78(21), pp.3322-3324, 2001
[3] E. Boyd, X. Cao, D. A. Moran, and et. al., *12th GAAS Symposium-Amsterdam 2004*



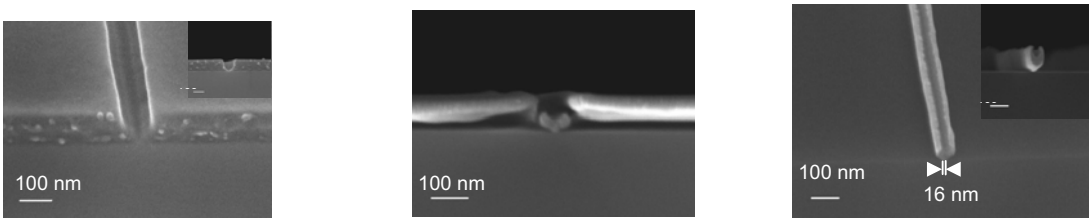
(a) (b) (c)

Fig.1 Schematic for fabricating a T-gate mold. (a) Duplicate high aspect ratio SiO2 grating on Si substrate by NIL, (b) comformally deposit SiNx by LPCVD, and (c) anisotropically etch down the SiNx layer to achieve an inverted T-shaped mold.



(a) (b) (c)

Fig. 2 SEM images of (a) SiO2 footprint on Si mold substrate fabricated by nanoimprint and HF size reduction etching, (b) Conformal deposition of SiNx on the SiO2 nanowires, and (c) T-gate imprint mold formed after RIE etching (the scale bar in the insertion is 30nm).



(a) (b) (c)

Fig. 3. SEM image of (a) imprinted resist using a composition mold with T-gate protrusion, (b) cross section of metal T-gate after Au evaporation before lift-off, and (c) free standing 16 nm Au T-gate after lift off (the scale bar in the insertion is 100nm).