Improvement of high resolution lithography capabilities by using amorphous carbon hard masks

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The ability to perform high resolution nanostructures is fundamental to develop new microelectronic devices. At present, some process integration problems appear due to resist thickness diminution induced by critical dimension down scaling. In this study, amorphous carbon hard masks [1] with a thin oxide capping layer were added on our structure in order to suppress resist thickness limitations and extend e-beam capabilities.

Carbon layer offers new possibilities for improving high resolution lithography because of the fact that very thin resist films (below 100nm) can be exposed and etched. Thanks to a lower resist thickness budget to transfer into the underneath layer, ultimate resolution as well as the pattern collapse for dense lines are expected to be improved. Furthermore, carbon hard masks can be trimmed in order to reduce initial e-beam lithography critical dimensions (Fig. 1) [2].

For this study, we have used chemically amplified resists (CAR) which have the advantage of being fully compatible with e-beam and optical lithography with high sensitivity and resolution [3]. E-beam exposures were achieved on a gaussian electron beam lithography equipment (Leica VB6UHR from Vistec) operating at 100 KV and DUV exposures on an ASML stepper with a wavelength of 248 nm.

Finally, we have succeeded in achieving 30nm dense line arrays (Fig.2). This technique was also used to pattern metal oxide semiconductor (MOS) transistor gates by hybrid lithography (e-beam/DUV) (Fig. 2) [4]. Thus, 20nm MOS transistor gates were achieved and electrically tested (Fig. 2) [5], and by improving our etching process we have obtained 7nm MOS transistor gates.

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[1] Kevin A. Pears, Microelectronic Engineering 77 (2005) 255-262.
[2] Xusheng Wu, Philip C. H. Chan, Shengdong Zhang, and Mansun Chan, Electron Devices and Solid-State Circuits, IEEE Conference on 19-21 Dec. 2005 p. 781 - 784
[3] S. Landis, S. Pauliac and al, Jap. J. of App. Phy., Vol. 43, No 6B, 2004, pp. 3974-3980.
[4] S. Pauliac, S. Landis, J. Foucher, J. Thiault, Microelectronic Engineering 83 (2006) 1761-1766
[5] S. Pauliac-Vaujour, P. Brianceau, O. Faynot et al., J. Vac. Sci. Technol. B, Vol. 25, Issue 6, pp. 2030-2033 (2007)

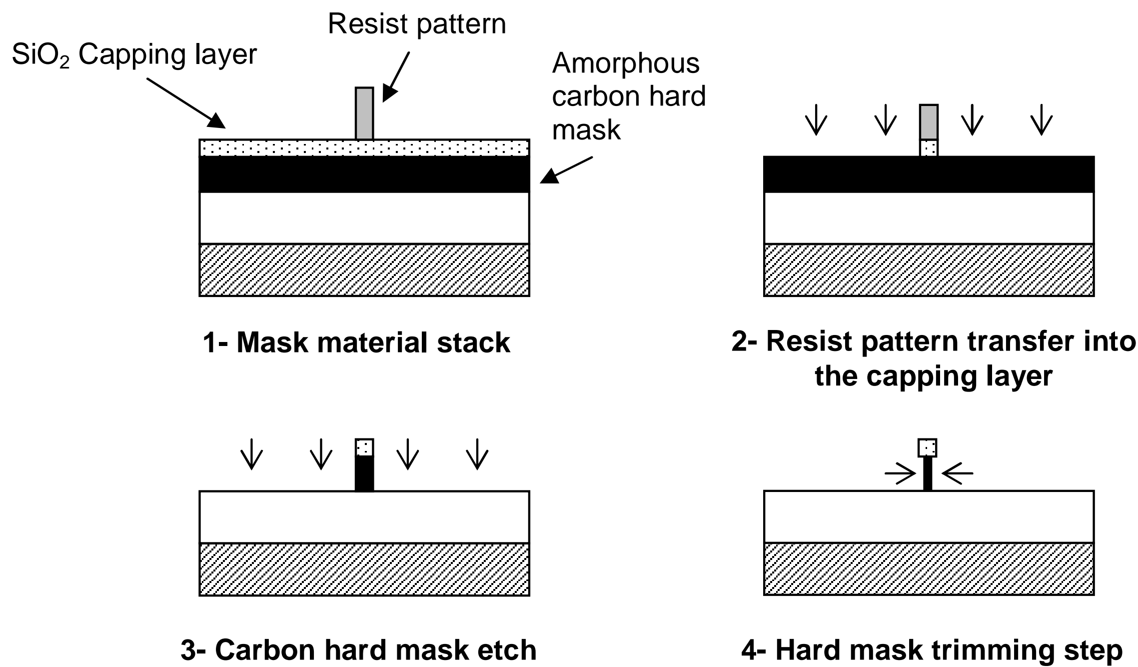

Fig. 1: Successive steps of the carbon hard mask trimming process

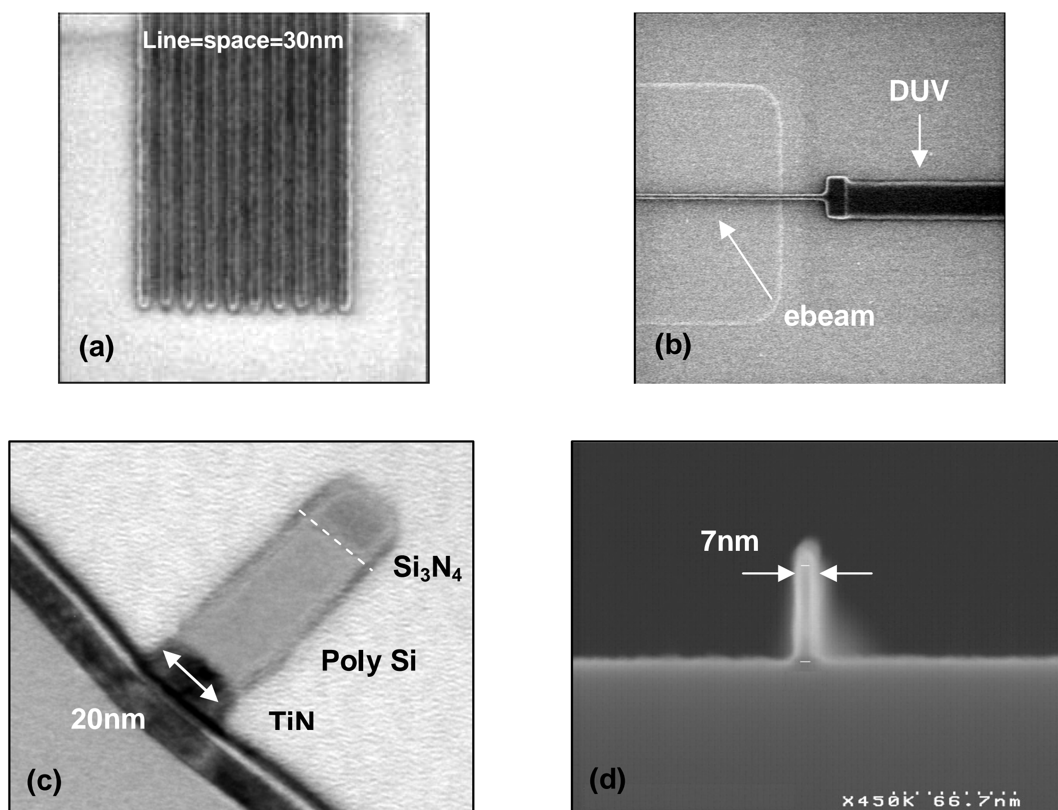

Fig. 2: Results. (a) SEM view of a 30nm dense line array, (b) SEM view of a resist gate pattern achieved by hybrid lithography, (c) TEM image of a 20nm MOS transistor gate (with carbon hard mask trimming), (d) SEM view of a 7nm MOS transistor gate.