Study of machine to machine overlay error for sub-60-nm memory devices

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According to the 2006 international technology roadmap for semiconductors, the overlay budget of 60-nm memory devices is 11 nm. To meet such a tight requirement, the total overlay error budget should be controlled carefully. It turns out that scanner contributions due to machine to machine overlay error (MMO) are nearly half of the total overlay error budget. In a conventional way, overlay errors are corrected by 10 linear terms: offset x, y, wafer rotation x, y, wafer magnification x, y, shot rotation x, y, shot magnification x, y. Especially for the shot correction, an average value is applied commonly for all shots. MMO cannot be compensated by only linear correction to meet such a tight specification any longer. In this paper, a grid matching strategy through per-shot-correction (PSC) is investigated so that scanner contributions are minimized. In PSC, shot correction is implemented for each shot with different correction parameter values. By matching wafer grids from machine to machine, overlay budget is confirmed for sub 60 nm memory devices.

Key words: semiconductor, photolithography, overlay, alignment

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