Line Edge Roughness Impacts on Overlay

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Overlay control is one of the most critical requirements for manufacturing integrated circuits, and the overlay tolerance for the front end of line is very close to single digit. For the 32 nm node, the 2006 International Technology Roadmap for Semiconductor (ITRS)[1] specifies that overlay (3σ) must be less than a mere 6 nm. In this paper, we will present a fundamental study of the effect of line edge roughness (LER) on overlay and its possible implications on design rules.

Currently overlay is measured on large features that are tens of microns in size, and such measurements may not be a good representation of the overlay of individual features in the circuit, which are typically shorter than 100 nm these days. Although people have been working hard to improve the overlay metrology and to capture the so-called in-die overlay [2-3], the target size is still on the micron-scale. The actual overlay for devices can be larger than the measured one, and line edge roughness is one of the reasons.

On the device level, the center of a feature on one layer may be different from the center of the to-be-aligned feature on another layer due to LER. This LER-induced center-to-center overlay $\sigma_{overlay-c}$ is found to be the following:

$$\sigma_{overlay-c} = \frac{1}{2}\sqrt{\sigma_{CD1}^2 + \sigma_{CD2}^2}$$

Where σ_{CD1}^2 and σ_{CD2}^2 are the LER-induced critical dimension (CD) variation for to-be-aligned features on two layers. Figure 1 shows an example of simulation results on how the LER-induced center-to-center overlay varies with measurement length for LER (3σ) of 4 nm and correlation length of 25 nm. It can be seen that when the measurement length is 5 μm, the measured LER-induced overlay (3σ) error is 0.3 nm. However, if the measurement length can go down to 100 nm, the measured LER-induced overlay (3σ) error is about 1.7 nm which is closer to the actual center-to-center overlay on the device level.

In many cases, the edge-to-edge overlay is more relevant, and the LER-induced edge-to-edge overlay is directly proportional to the sum of variances from to-be-aligned edges on different layers. We will present our analytical study in detail, and the impact on design-rule related issues will be addressed and discussed.

References:
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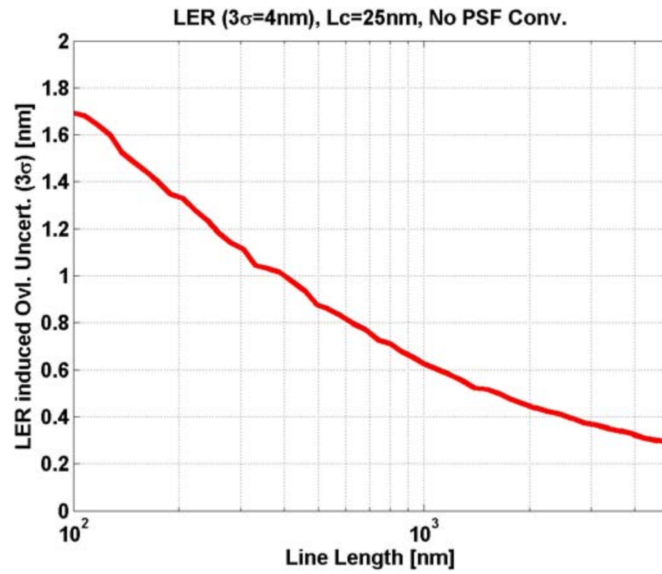

Figure 1. The LER-induced center-to-center overlay with respect to the measurement line length for $LER(3\sigma) = 4nm$ and correlation length of 25 nm.