

Impact of plasma etching processes on 193 nm photoresist: etch resistance and Line Width Roughness

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Successful pattern transfer by lithography and plasma etching requires minimal mask erosion, degradation and roughening. However, going to 193 nm based lithography in manufacturing several years ago brought new issues such as poor etching resistance of the photoresist masks during front end and back end processes. Indeed, the transition from 248 nm to 193 nm exposure sources has introduced significant changes in the composition of the photoresist (PR), including the removal of all aromatic functional groups due to their excessive absorption at 193 nm. Due to these important chemical changes, 193 nm PR not only exhibit poor etch resistance but are also thinner limiting strongly the 193 resist budget. Moreover, it was observed that 193 nm PR present severe surface roughening after plasma etching that can lead to wiggling and striations, impacting directly the resist Line Width Roughness (LWR). The critical issue is that PR degradation during plasma etching processes is possibly transferred into the underlayers, resulting in a polysilicon gate LWR above the requirements of the ITRS (1.4nm at 3σ for the 45 nm technological node). So far there is no real understanding on how different manufacturing operations may impact the resist roughness and its transfer into complex stacks of materials. In this work patterned and blanket 193 nm PR have been exposed to typical plasma etching processes involved in gate stack etching. In this work, we will show first correlations between etch rates (measured by ellipsometry), chemical analyses of the resist surfaces after plasma exposure (FTIR, XPS) and physical modifications on blanket resist substrates (using DSC and AFM), in order to better understand the etching and roughening mechanisms of typical 193 nm resists. The evolution of the patterned resist LWR and its transfer into the underlayer during the subsequent lithography and plasma etching steps are investigated by CD-AFM. We demonstrate that the resist LWR measured before etching is a key parameter in the final polysilicon LWR. Different plasma treatments applied to the 193 nm photoresist patterns prior to all the following plasma etching steps can reinforce the 193 nm resist etch resistance and smooth the resist sidewalls thus reducing the LWR of the polysilicon gate. Our results also show that resist faceting induced by the ion bombardment plays a key role in the smoothing or roughening of the resist and pattern sidewalls.