Electron-Transparent Cantilevers for TEM Visualization of Nanodevices

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For obtaining quantitative information about the size and structure of nanoelectronic devices on nanometer length scales, transmission electron microscopy (TEM) is generally regarded to be the best method available.[1] At the same time, TEM is known for its difficult sample preparation as compared with other methods. These difficulties are especially challenging when one wishes to image a nanoscale device for which one needs to arrange the electron transparency precisely where the device of interest is located, and must do it without destroying the device. Although site-specific methods for such sample preparation *a posteriori* exist,[2] a better way is to array the nanodevices directly on electron-transparent material so that any electrically interesting devices can readily be examined at any time using TEM. In this paper, we report on a new technique that allows the fabrication of nanodevices on electron-transparent cantilevers, and we illustrate it by applying it to the characterization of gold nanocluster devices.

The devices of interest consist of gold nanoclusters self-assembled between closely spaced electrodes. Such devices exhibit strongly nonlinear characteristics whose origins remain uncertain.[3] Our basic approach is to form SiN cantilevers that are supported by an InP substrate. Our process consists of the following steps: First, 100 nm thick PECVD SiN is deposited on an InP wafer, where the latter was chosen because of the precision with which this material can be cleaved. Nanofinger electrodes with gap sizes ranging from 15 nm to 40 nm are fabricated using e-beam lithography and metal lift-off. The devices were aligned so that later the wafer could be cleaved leaving them all very close to a chip edge. The layout also included metal lines running to bonding pads set some distance away from the future cantilevers. Next, the cantilever regions are defined in the SiN using e-beam lithography and reactive ion etching. V-shape grooves are then cut into the InP using wet HCl etching.[4] A set of these grooves is placed within a few microns of the devices, and then used to guide the cleaving of the sample. A final HCl-based etch forms an undercut which defines the device-bearing cantilevers on the edges of the chip. This geometry is shown at the chip level in Fig. 1 and at the cantilever level in Fig. 2. For our work to date, the cantilevers were 100 nm in thickness which combines mechanical strength with the needed electron transparency to make TEM inspection easy.

To complete the devices they are immersed in various solutions that result in the self-assembly of nanoclusters between the nanofinger electrodes as described in reference 3. The electrical characteristics of one such device is shown in Fig. 3, and it clearly exhibits the expected nonlinearity. The TEM image of this same device is shown in Fig 4, and it demonstrates the power of our technique. From this Figure we can see not only the randomness of the nanocluster assembly, but also that it seems very likely that all the current is carried by the very few clusters interposed between the nanofingers. The value of these special substrates is therefore evident, and it is clear that this technique could be used for many other nanodevices including potentially molecular electronic devices.

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[3] A.W. Snow et al, J. Mat. Chem.12, 1222 (2002).
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[Figures]

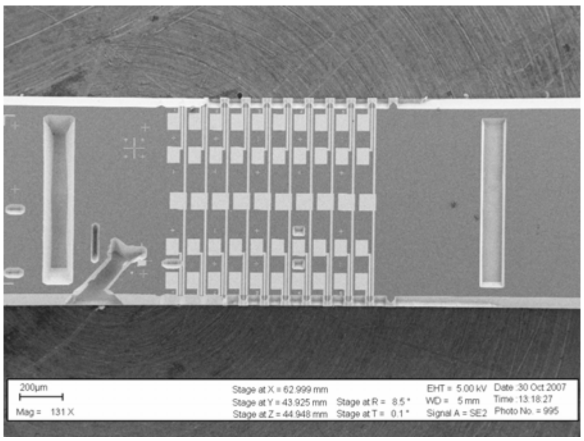

Figure 1. SEM image of nanofinger devices at the chip level.

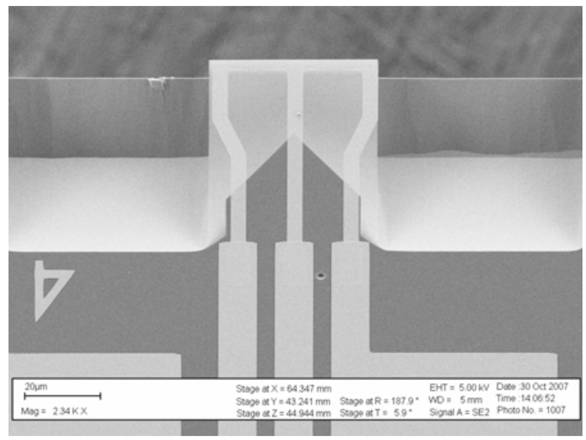

Figure 2. SEM image of a SiN cantilever with two nanofinger devices.

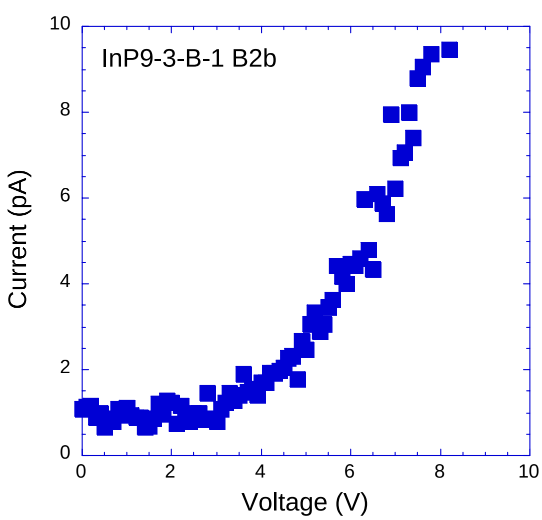

Figure 3. Current and voltage characteristic of gold nanoclusters self-assembled between closely spaced electrode.

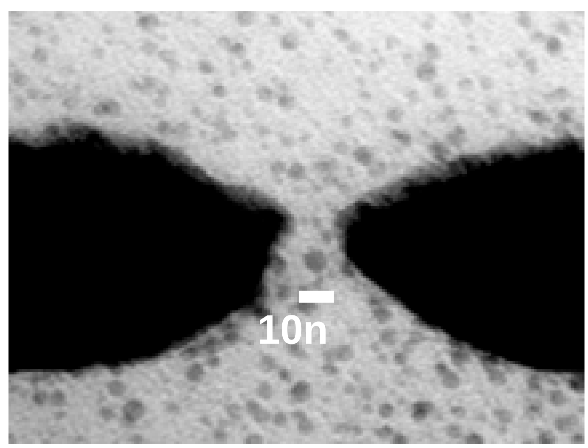

Figure 4. TEM image of gold nanoclusters self-assembled between closely spaced electrode.