Controlled chemical mechanical polishing of polysilicon and silicon-dioxide for Si based single-electron device with oxide tunnel barriers

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We present a method to fabricate a Si based single-electron transistor (Si-SET) using lithography, dry-etching and chemical mechanical polishing (CMP). Previously reported results on Si-SETs[1,2] show that these devices have excellent long term charge stability, the obligatory feature for any practical use of SET devices. Si-SETs operating at room temperature have been reported in the literature, but these devices suffer from a number of problems due to uncontrolled dot size and tunnel barrier thickness[3]. Our method produces an SET with a well-defined geometry of the dot and, most importantly, a high quality well-controlled tunnel oxide. A simplified description of the fabrication is as follows. The device layer (~50 nm thick) of a SOI wafer is patterned by electron-beam lithography (EBL) and high selectivity inductively coupled plasma (ICP) etch to form thin Si ribs (~20-40 nm wide) and an adjacent gate on the buried oxide (BOX). Silicon dioxide is deposited on the sample with a thickness greater than that of the Si rib and planarized using CMP to expose the top of the ribs. The SET island is defined by writing lines (~20-40 nm wide) by EBL to perpendicularly intersect the Si rib. The exposed part of the Si rib is etched up to the BOX using the same high selectivity ICP etch. An ultrathin thermal oxide (<1.5 nm) is grown on the sidewalls of the etched pit in the Si rib. LPCVD polysilicon is deposited on the sample, filling the pit and a final CMP step removes the overburden of polysilicon, leaving only that in the pit. A 3-dimensional representation of completed device is shown in Fig. 1.

We present the initial results derived from the characterization of the different fabrication steps and the device. The degenerately doped Si ribs are conductive at 4.2K indicating no carrier freeze out. The ultrathin thermal SiO_2 is grown in a rapid thermal processor (RTP) system and characterized using I-V measurements. The fabrication method introduces CMP as a key processing technique in the production of nanometer scale features for SETs[4]. Fig. 2 shows controlled CMP of patterned structures to form a 20 nm thick layer of polysilicon. Fig. 3 shows an AFM image of the partially completed device. Our calculations, based on the device properties, suggest a charging energy in excess of 4 meV, resulting in operation temperatures above 10K.

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[3] Y. Takahashi *et al.*, Electronics Letters, **31(2)**, 136-137 (1995).
[4] V. Joshi *et al.*, J. Vac. Sci. Technol. A **25(4),** Jul/Aug (2007).

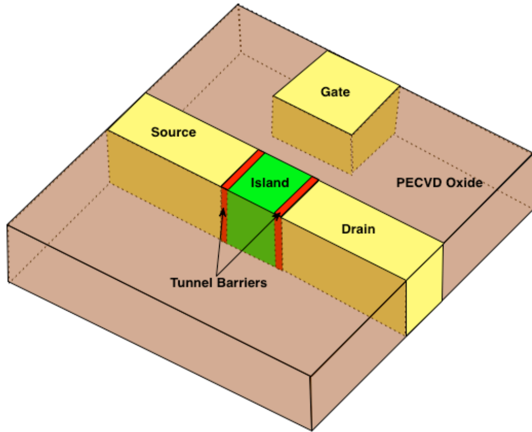

Fig 1: A 3-D pictorial representation of the proposed device

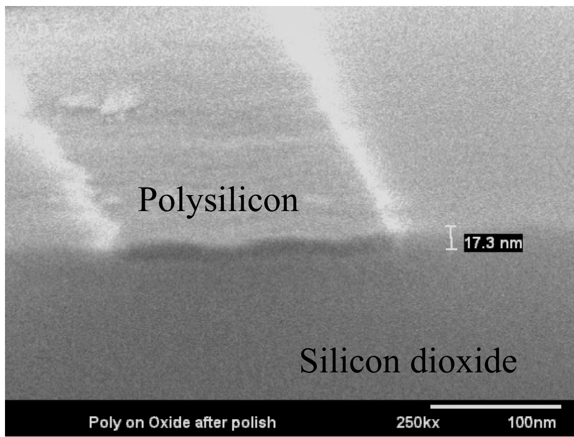

Fig 2: < 20 nm thin polysilicon channel fabricated by CMP

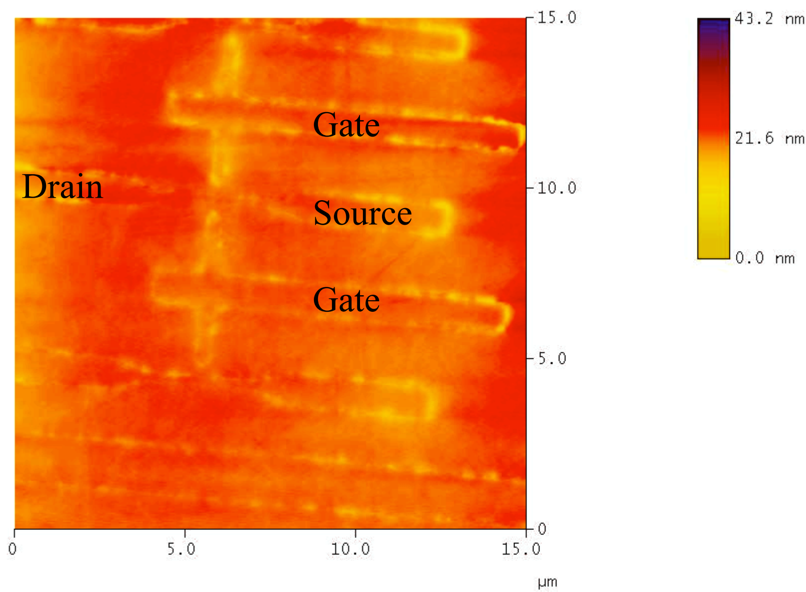

Fig 3: AFM surface scan of the structure after the oxide CMP to reveal the embedded Si rib structures.