Hybrid high resolution lithography (e-beam/DUV) and etch process for achieving stacked nanowire MOSFETs

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Stacked nanowire MOSFETs offer an excellent electrostatic control combined with a high on-current (I_{ON}) [21]. Furthermore, it was demonstrated that their power consumption could be reduced by using independent double-gate MOSFETs [2].

The stacked nanowire transistor fabrication is highly complex with regards to lithography and etching (Fig. 1). Active area definition is the most critical lithography level. These very dense line patterns are achieved by hybrid lithography (e-beam/DUV) (Fig. 2), via the use of chemically amplified resists (CAR). CARs have the advantage of being fully compatible with both types of exposure (e-beam and DUV) [3-5]. However, in order to achieve features of critical dimension 20nm, the resist thickness must no exceed 100nm (aspect ratio of 5, [6]), which is not sufficient to pattern Si/SiGe multilayer stacks of thickness 250nm.

Two ways are explored in order to pattern 20nm active area stacked nanowire MOSFETs. On one hand, resist patterns with a large critical dimension (45nm) are used in order to increase resist thickness up to about 280nm. Subsequently, a resist trimming is performed before Si_3N_4 and multilayer etching (Fig. 3). On the other hand, amorphous carbon hard masks with a thin oxide capping layer are added to the structure to suppress resist thickness limitations and extend high resolution lithography capabilities [6, 7].

The best results so far were obtained using the first of these two techniques, which yielded 25nm stacked nanowire MOSFETs (Fig.3).

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[1] T. Ernst et al., IEDM Techn. Digest 2006, p.997
[2] Y. X. Liu et al., IEEE Int. SOI Conf. 2005, p. 219
[3] S. Pauliac, S. Landis, J. Foucher, J. Thiault, Microelectronic Engineering 83 (2006) 1761-1766
[4] S. Landis, S. Pauliac et al, Jap. J. of App. Phy., Vol. 43, No 6B, 2004, pp. 3974-3980
[5] S. Landis, S. Pauliac, J. Foucher, J. Thiault and F. de Crecy, J. Vac. Sci. Technol. B 23, 2733 (2005)
[6] S. Pauliac-Vaujour, P. Brianceau, O. Faynot et al., J. Vac. Sci. Technol. B, Vol. 25, Issue 6, pp. 2030-2033 (2007)
[7] Kevin A. Pears, Microelectronic Engineering 77 (2005) 255-262

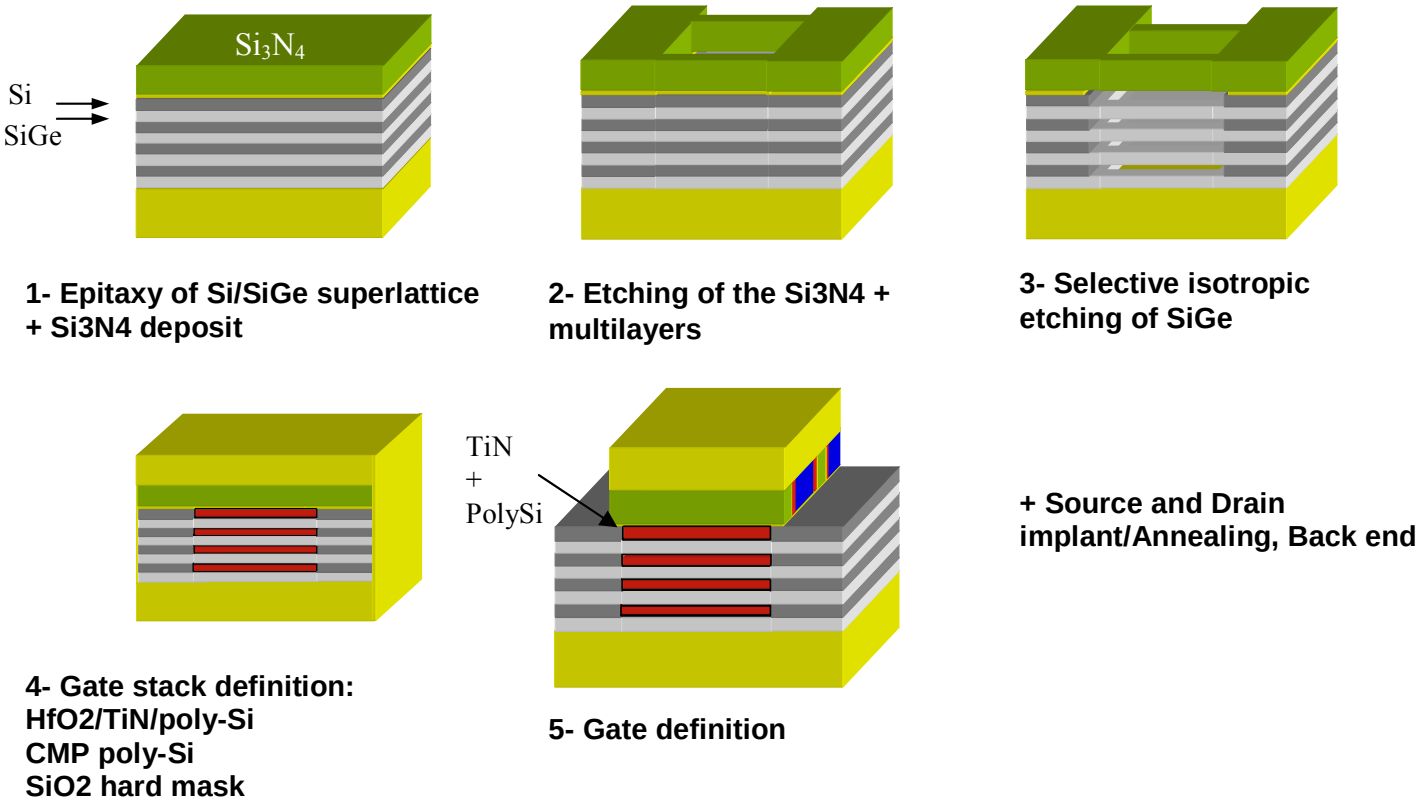

Fig. 1: Stacked nanowire MOSFET process flow

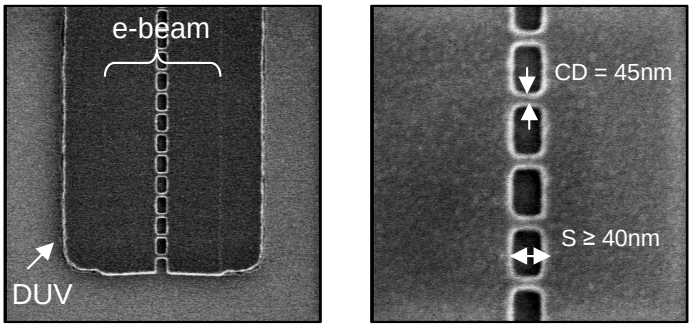

Fig. 2: hybrid lithography for patterning the Si_3N_4 + multilayers (CD: critical dimensions, S: space)

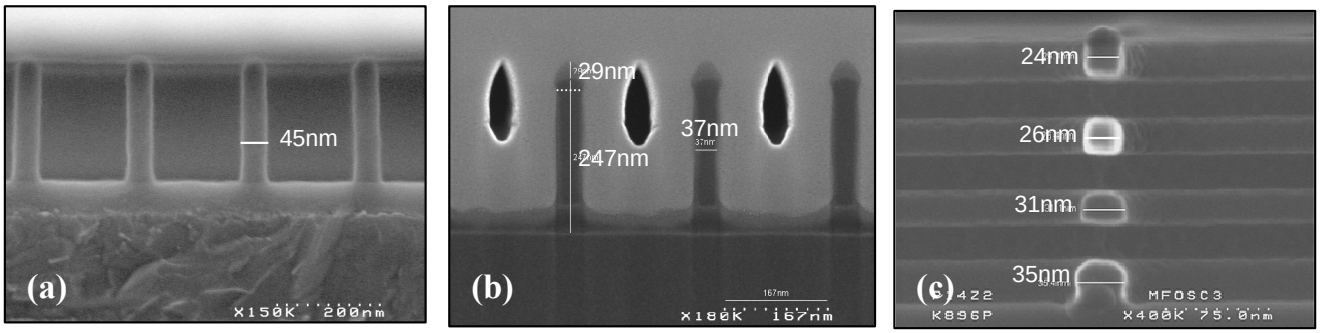

Fig. 3: Results. (a) resist pattern before trimming and etching, (b) after resist trimming, Si_3N_4 and multilayer etching, (c) after isotropic etching of SiGe (with resist trimming).