Self-aligned asymmetric recess technique with e-beam lithography

Yumin Koh, Sungwon Kim, and Kwangseok Seo
School of Electrical Engineering, Seoul National University,
San 56-1 Shillim-dong Kwanak-gu Seoul 151-742, Republic of Korea

InGaAs/InAlAs high electron mobility transistors (HEMTs) are considered to be one of the most promising devices for millimeter-wave applications because of their superior high frequency and low noise performances. In order to achieve higher frequency performance, it is necessary to improve cut off frequency (f_T) and maximum oscillation frequency (f_{max}). Generally, reducing gate length is to increase f_T, but to decrease f_{max} due to the increase of output conductance. For this reason, asymmetric recess technique is widely used to improve f_{max} with preserving high f_T, which is to widen the length of side-recessed region toward the drain. However, the conventional asymmetric recess usually uses four-layer resist[1] or slit patterns with a complicated process.[2]

In this work, we have developed self-aligned asymmetric recess, which is simpler than a conventional asymmetric recess because of utilizing only bilayer resist without any additional process step.

Fig.1 shows the process flow of EB lithography for bilayer resists, which consist of a bottom layer of ZEP520 and a top layer of UV5. After definition of the bottom layer, the top layer was exposed and then the wet chemical gate recess etching was performed.[3] Fig. 2 shows the SEM image of T-gate with asymmetric recess. It is found that the asymmetric recess profile was achieved because the wet etch rate to drain-side is higher than that to source-side as shown in Fig. 3. This indicates that EB exposure of the top layer might facilitate the wet etch rate of EB exposed region.

This self-aligned asymmetric recess technique is the novel process that makes an asymmetric recess without any additional pattern or EB lithography. Therefore, this has advantages of simple and effective process to improve frequency performance of InGaAs/InAlAs HEMTs.

[1] R. Grundbacher, I. Adesida, Y. C. Kao, and A. A. Ketterson, J. Vac. Sci. Technol. B **15**, 49 (1997)
[2] K. Shinohara, T. Matsui, Y. Yamashita, A. Endoh, K. Hikosaka, T. Mimura, and S. Hiyamizu, J. Vac. Sci. Technol. B **20**, 5 (2002)
[3] S. Kim, Y. Koh, and K. Seo, Electron. Lett. Vol. **43**, 16, pp. 895-897 (2007)

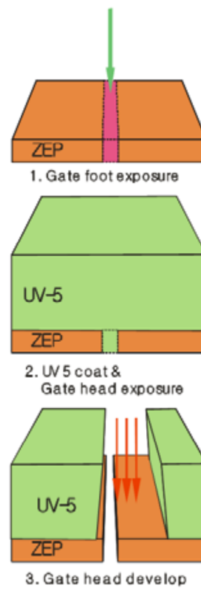

Fig. 1: The process flow of EB lithography for bilayer resists

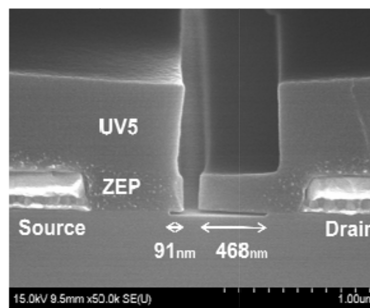

Fig. 2: The SEM image of T-gate with asymmetric recess

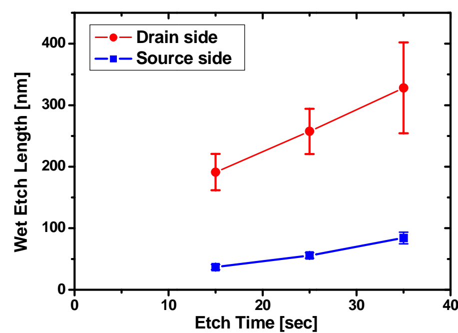

Fig. 3: Wet etch length as a function of etch time; source side (filled circle) and drain side (filled square)