Sub-50nm resolution surface electron emission lithography using nano-Si ballistic electron emitter

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In the microelectronics industry, a nanoscale lithographic technique is intensely required for future generation semiconductor devices at the sub-50-nm node and beyond. For this next generation lithography, the 1:1 electron stepper using a patterned surface electron emission source has many advantages because of its high throughput, fine patterning and simple electron optics.

In order to create deep sub-50nm patterns, the patterned surface electron emission source must emit electrons with small energy dispersion and small emission angle, since the energy distribution of electrons and emission angle strongly affects the electron beam spread which dominates the resolution of exposure.

In this work, we employed a nano-Si ballistic electron surface emitting device (BSD) as an electron emission source in a 1:1 electron stepper system. The simple design of the system is shown in Figure 1. A focusing magnetic field of 0.6T is provided with two magnets. An accelerating voltage is applied to the target wafer, and the focus is controlled by the adjustment of the strength of electric field. When the electrons were emitted from BSD with 40 nm-wide-lines emission area, the resulting exposed area on the wafer was approximately 40 nm-wide-lines pattern as shown in Figure 2. The structure of patterned BSD is indicated in Figure 3. The electrons are transported and accelerated by cascade tunneling between Si nanocrystals with reduced electron scattering probability due to quantum effects of nano-crystalline Si covered by SiO₂ thin layer.

We demonstrated a resolution of 40nm even in this low accelerating voltage condition of 5.7keV. The resolution will be improved to better than 20nm at the higher accelerating voltage because it directly depends on the field strengths. The 1:1 electron stepper system using BSD provides promising technique for the next generation lithography in the deep sub-50-nm scale.

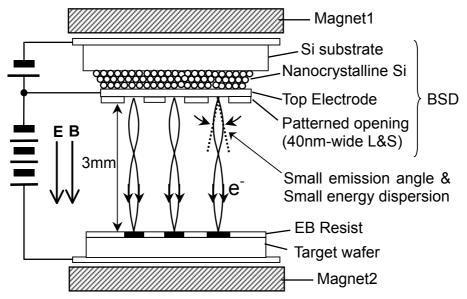


Figure 1. Schematic diagram of 1:1 electron stepper using BSD. The target wafer is positively biased (= 5.7 kV) and a coaxial magnetic field (= 0.6 T) is applied with two magnets.

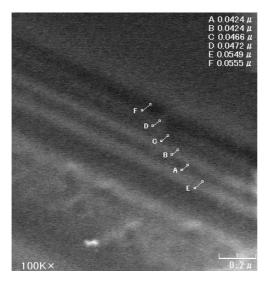


Figure 2. SEM Image of approximately 40nm-wide Line & Space pattern exposed on EB resist of the target.

Si nanocrystal (φ3-5nm) covered with thin oxide

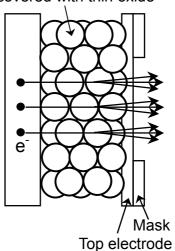


Figure 3. The structure of patterned BSD.