Self-Aligned Fabrication of 10 nm-Wide Asymmetric Trenches in Si for Heterojunction Tunneling FETs Using Nanoimprint Lithography, Shadow Evaporation, and Etching

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Traditional MOSFETs' source and drain, which are identical and symmetrically defined next to the gate, are fabricated simultaneously using a self-aligned method. However, such self-alignment becomes inapplicable in a heterojunction tunneling FET – a potential revolutionary transistor, where the source (a regrown SiGe in a trench) is completely different from the drain (doped Si). The asymmetric nano-trench must be precisely aligned to the gate within a few nanometers, making it extremely difficult, if possible, to be achieved using a conventional lithography alignment. To solve this problem, here we propose and demonstrate a novel, simple and reliable self-aligned method to fabricate a sub-10 nm wide asymmetric trench to only one side of the gate.

The key approach here (Fig. 1) is to use the gate as a shadow mask in a Cr oblique evaporation. After the evaporation, Cr will be anywhere on the substrate except for the shadow area behind the gate, and the width of shadow area can be controlled by the evaporation angle θ and the gate height H. Then Cr will be used as a mask for etching Si substrate and removed afterward.

To test the concept, we first fabricated Si gratings of 40 nm tall and 200 nm pitch (20 nm wide) on Si, using nanoimprint lithography (NIL), metal lift-off, and RIE (Fig. 2 (a)). Then a 10 nm thick layer of Cr was evaporated from an oblique angle θ of 20 degrees, creating a 13 nm-wide gap. A fluorine based RIE was used to etch a trench into the Si substrate. By varying H and θ, we were also successful to get nano-trenches with different widths. Fig. 3 shows 10 nm and 25 nm wide trenches self-aligned to 40 nm and 60 nm high Si gratings using θ=15 and θ=25 degrees, respectively.

We believe that beside semiconductor ICs, this simple, reliable, and effective self-aligned fabrication of sub-10 nm asymmetric trenches will have various applications in nanophotonics, nanobiotechnology and NEMS.

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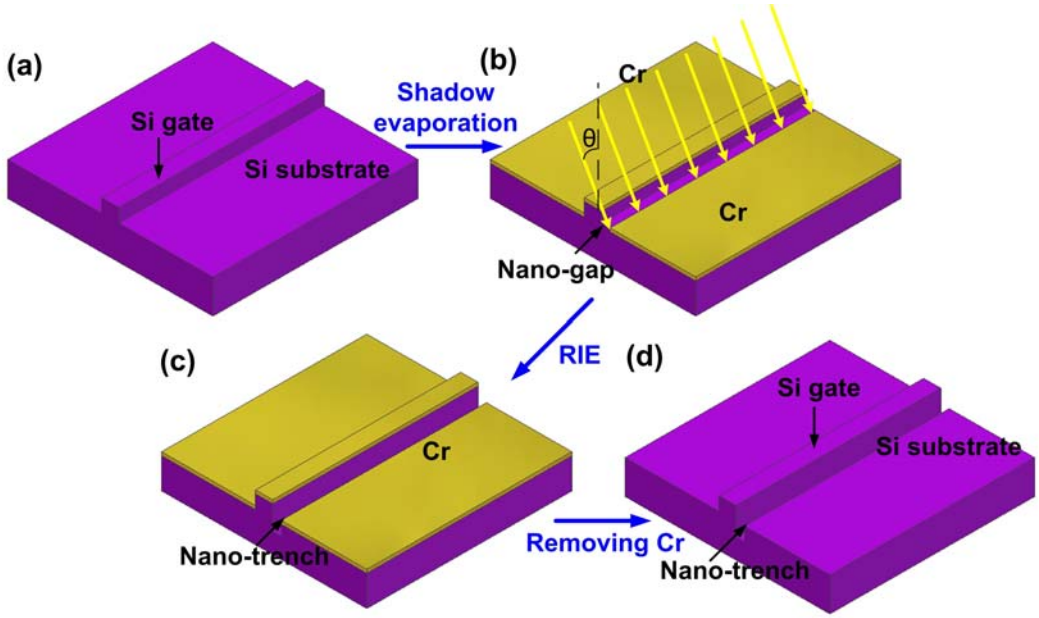

Fig. 1. A self-aligned fabrication process for an asymmetric nano-trench next to the gate: (a) a Si gate fabricated; (b) the gate is used as a shadow mask for an oblique evaporation of Cr; (c) Etch an asymmetric trench by RIE; and (d) remove Cr.

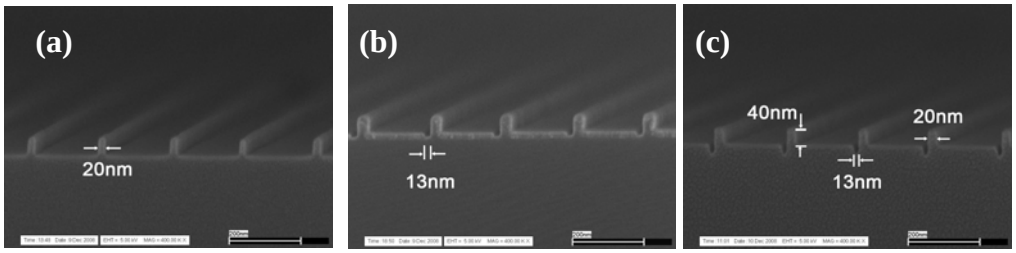

Fig. 2. 13 nm-wide self-aligned asymmetric nano-trenches: (a) 20 nm-wide, 40 nm-high Si gratings fabricated by NIL, Cr liftoff, RIE and removing Cr mask; (b) 13 nm-wide gaps created by Cr shadow evaporation at an oblique angle of 20 degrees; (c) 13 nm-wide asymmetric trenches in Si after RIE and removing Cr.

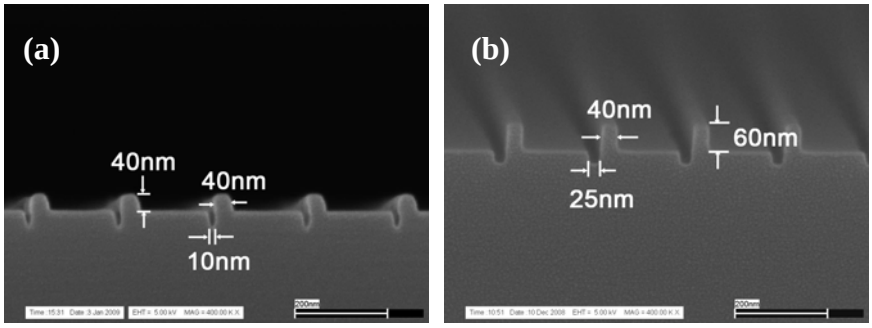

Fig. 3. 10 nm- and 25 nm - wide self-aligned asymmetric nano-trenches next to the gate (Cr mask was removed): (a) 10 nm-wide trenches self-aligned to 40 nm-wide, 40 nm-high Si gratings. (b) 25nm-wide trenches self-aligned to 40 nm-wide, 60 nm-high Si gratings.