Design for EB (DFEB), a Novel Approach to EBDW throughput enhancement for volume production

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Rising mask cost threatens the profitability of future custom LSI especially for 65nm node and beyond. EBDW with character projection (CP) function is one of the most promising technologies to the solution of this issue. We already established basic technology for 65nm [1].

However drastic improvement of throughput is indispensable for the extent to volume production. Multi-beam approach of MCC [2] is effective but is not sufficient to attain higher throughput of more than 5 Wph. The ordinal shot count reduction with CP is done by the recognition of repeatability of physical design data. Nevertheless the reduction efficiency is limited to around 4 times.

In this paper we report the new concept of DFEB (Design for Electron beam) which enables much higher shot count reduction rate of more than 10 times.
In this method we create the EB friendly design layout data by tracing back to upstream design flow. A DFEB cell library and a DFEB mask data are created from the original cell library in CP friendly manner as shown in Fig.1. DFEB customization includes (1) partial CP conversion, and (2) common base cell concept. These techniques virtually increase the number of characters on a stencil so that the shot count can be further reduced. Starting with RTL DFEB customized net-list is synthesized with this library and optimized to minimize the estimated shot count, while keeping the circuit performance. DFEB layout data and stencil design data are created in this step. With this design flow, we can expect drastic improvement of shot count reduction efficiency. In practice we estimated the shot count reduction efficiency with 65nm Low Power production sample design. The shot count reduction data are shown in Fig.2. The reduction rate of around 10 times is attained. The layout area penalty of standard cell part in DFEB design is around 10 % as shown in Fig.3. Considering standard cell utilization and standard cell area occupancy of the chip, the layout penalty at chip level is permissibly low for practical use. The resolution degradation of large area CP exposure is one of the worries for practical use. We confirmed, however, enough resolution potential by actual 45nm node printing experiment. Fig.4 shows the SEM images of exposed patterns with 45nm node stencil mask. The diffusion, poly, contact and metal patterns were finely performed.
In conclusion we proved the usability of DFEB scheme for device production.

Otherwise, the definition of condition concerning coulomb interaction and the establishment of partial CP methodology are important in practical use. We also report these technical outputs.

[1] T. Maruyama et al., Proc. of SPIE Vol.6921 69210H (2008)
[2] A.Yamada et al., J. Vac. Sci. Technol. B Vol. 26, pp. 2025-2031 (2008)

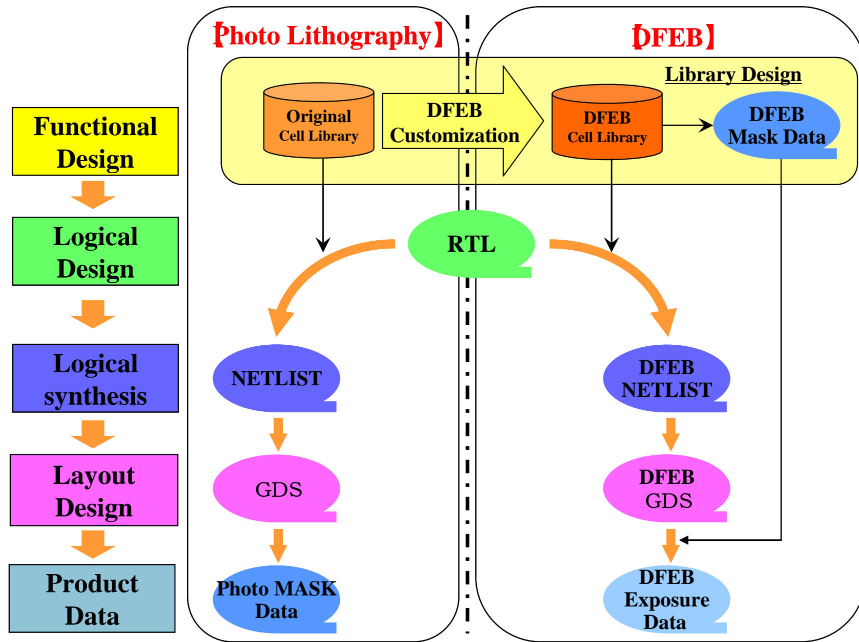

Fig 1: DFEB LSI Design Flow

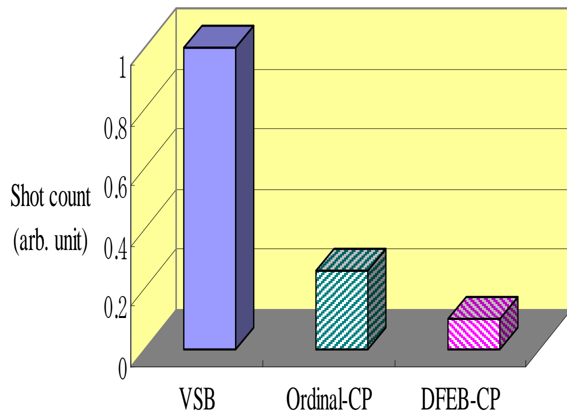

Fig2: Shot count reduction with DFEB

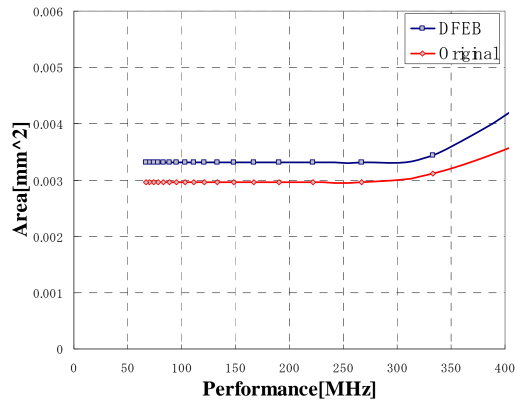

Fig3: Area penalty in DFEB design

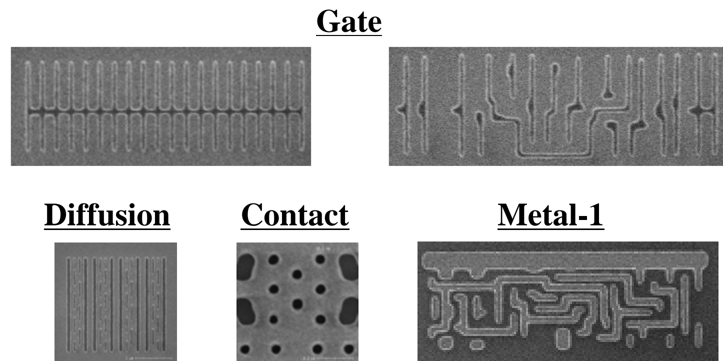

Fig4: SEM images of 45nm stencil exposed patterns