[Invited] Overcoming the Patterning Challenges of Extreme k_1 Imaging

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Historically, lithographic scaling was driven by both improvements in wavelength and numerical aperture. Recently, the semiconductor industry completed the transition to 1.35 NA immersion lithography and consequently the industry's research teams have focused on enabling double exposure (DE) and double patterning (DP) techniques as means to circumvent the limitations of single exposure diffraction[1]. Recently, the extendibility of a series of double exposure and double patterning solutions that enable scaling of logic constructs by decoupling the pattern spatially through mask design or temporally through innovative processes has been demonstrated at $<0.28\ k_1$ [2].

As resolution pushes beyond the 0.25 k_1, the industry is looking for the next solution. Currently, two leading candidates for methods of increasing pattern density are Double Patterning[3,4,5] and EUV Lithography. While EUV remains a major focus of the industry's lithography community, the dramatically reduced wavelength enables high-k_1 imaging at the 22nm and 15nm node and imparts more traditional design constraints. In this paper, we will focus on double patterning options and their challenges. Collectively, double-patterning is a set of techniques that use conventional optical lithography to reduce the effective pitch with the use of innovative processes. In particular, pitch-split double exposure techniques are under development as are self-aligned double patterning techniques[6]. Overlay[7] and design-sensitivity are key challenges for double-patterning technology. While at this point there is no clear winner, EUV and double patterning remain the two leading contenders for logic manufacturing.

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