High aspect ratio fabrication process for 3D nanowire gate-all-around (GAA) and double-gate (ΦFET) transistors

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Stacked nanowire metal oxide semiconductor field effect transistors (MOSFETs) with gate-all-around (GAA) offer an excellent electrostatic control combined with a high on-current (I_{ON}) [1]. This architecture is a real candidate for sub-32nm MOS transistors [2]. Furthermore, it was demonstrated that their power consumption could be reduced by using independent double-gate MOSFETs (ΦFET) [3].

The stacked nanowire transistor fabrication is highly complex with regards to lithography and etching (Fig. 1). Active area definition is the most critical lithography level. These very dense line patterns are achieved by hybrid lithography (e-beam/DUV) (Fig. 2), via the use of chemically amplified resists (CAR) which have the advantage of being fully compatible with both types of exposure (e-beam and DUV) [4-6]. However, in order to achieve features of critical dimension 20nm, the resist thickness must not exceed 100nm (aspect ratio of 5 [5]), which is not sufficient to pattern Si_3N_4 and Si/SiGe multilayer stacks of thickness 250nm.

Two ways are explored in order to pattern 20nm active area stacked nanowire MOSFETs. On one hand, resist patterns with a large critical dimension (45nm) are used in order to increase resist thickness up to about 280nm. Subsequently, a resist trimming is performed before Si_3N_4 and multilayer etching (Fig. 3) [5, 7]. On the other hand, amorphous carbon hard masks with a thin oxide capping layer are added to the structure to suppress resist thickness limitations and extend high resolution lithography capabilities [6, 8].

The best results so far were obtained using the first of these two techniques, which yielded 18nm stacked nanowire MOSFETs with gate all around (Fig.4). Furthermore, for the first time [9], we have succeeded in achieving sub-20nm ΦFET devices (Fig.5).

[1] T. Ernst et al., IEDM Techn. Digest 2006, p.997
[2] A. Hubert, C. Dupré, T. Ernst, S. Pauliac et al., ECS Trans. 13, (1) 195 (2008)
[3] Y. X. Liu et al., IEEE Int. SOI Conf. 2005, p. 219
[4] S. Pauliac, S. Landis, J. Foucher, J. Thiault, Microelectronic Engineering 83 (2006) 1761-1766
[5] S. Pauliac-Vaujour et al., J. Vac. Sci. Technol. B26(6), p2583 Nov/Dec 2008
[6] S. Pauliac-Vaujour, P. Brianceau, O. Faynot et al., J. Vac. Sci. Technol. B, Vol. 25, Issue 6, pp. 2030-2033 (2007)
[7] S. Barnola et al, ECS Transactions, 16 (10) 923-934
[8] Kevin A. Pears, Microelectronic Engineering 77 (2005) 255-262
[9] C. Dupré et al., IEDM 2008 (in press)

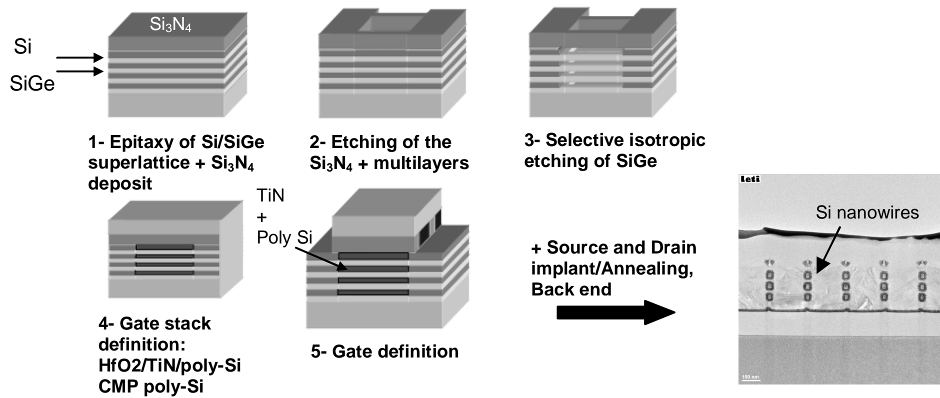

Fig 1. Stacked nanowire MOSFET (with gate-all-around) process flow

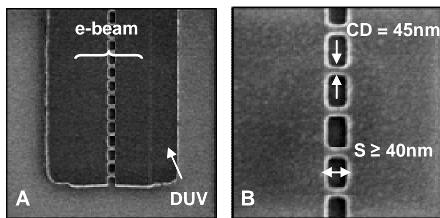

Fig. 2: Top SEM views of hybrid lithography for patterning the Si_3N_4 + Si/SiGe multilayer (CD: critical dimensions, S: space)

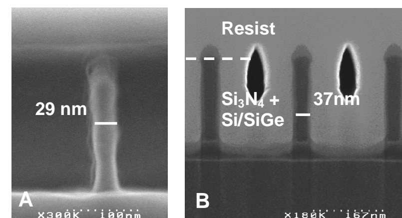

Fig. 3: Cross sectional SEM images of resist patterns after trimming (A) and after Si_3N_4, Si/SiGe etching (B).

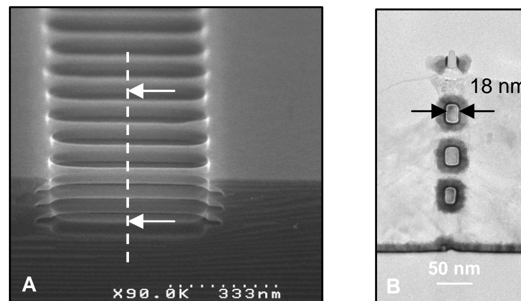

Fig. 4: SEM image of Si stacked nanowires (A), Cross sectional TEM view of sub-20nm nanowires (B)

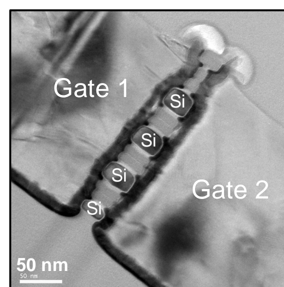

Fig. 5: Cross sectional TEM image of a ΦFET transistor.