Fully self-aligned process for fabricating 100 nm gate length enhancement mode GaAs MOSFETs

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Future scaling of CMOS, driven by cost-per-function reduction, may require high mobility channel materials based on III-V semiconductors to enable continued scaling [1]. As a result, "silicon-like" process modules are required for III-V MOSFETs if they are to be seriously considered for future CMOS applications. This work reports a process flow, which has enabled the first demonstration of functional, fully self-aligned 100 nm enhancement mode GaAs MOSFETs with metal gate and SiN sidewall spacers. The flow uses blanket metal and dielectric deposition and low damage dry etch modules, with no critical dimension lift-off processes required. The process flow described here is generic to any gate dielectric or underlying III-V semiconductor material, but in this work, is demonstrated using flatband-mode III-V MOSFETs with a GaO/GaGdO (GGO) high-κ gate dielectric stack and 10 nm $In_{0.3}Ga_{0.7}As$ high electron mobility channel as this structure has previously produced relaxed geometry high performance III-V MOSFETs using more conventional compound semiconductor processing techniques [2]. The full process flow combines a number of new low damage modules including a SF_6/C_4F_8 based platinum dry etch process with evidence of chemical mechanisms and the first demonstration of dry etching GaGdO in a $SiCl_4/SF_6$ chemistry. Initially, metal gates are formed by blanket deposition of a 3 nm platinum film using electron beam evaporation followed by a 240 nm thick sputter deposited layer of tungsten. Platinum was chosen as the gate contact as a high work-function metal is required to obtain a positive threshold voltage. The 100 nm gates were defined in NEB31 negative tone resist by electron beam lithography. The resist pattern was transferred to the tungsten layer by dry etching in an SF_6/C_4F_8 chemistry and then to the platinum layer with a low damage SF_6/C_4F_8 based dry etch. Following gate definition, a conformal layer of 300 nm SiN was deposited at room temperature by inductively coupled plasma chemical vapor deposition. 70 nm sidewall spacers were formed by anisotropically dry etching the SiN layer in an SF_6/N_2 chemistry. Source and drain contacts were formed by first opening a large resist window centered around the gate and dry etching the exposed GGO in a $SiCl_4/SF_6$ chemistry. Subsequently, a AuGeNi based ohmic contact metallization was deposited everywhere. To be silicon compatible and Au-free, this ohmic contact metallization could be replaced in future with a PdGe-based contact metallization. To define individual source and drain contacts, the wafer was planarized with resist which was etched back using a dry etch O_2 process to expose the ohmic contact metal on top of the gate (Fig 1) which was removed by $Ar/O_2/SF_6$ reactive ion etching (Fig 2). Finally, the wafer was rapid thermal annealed to form low resistance ohmic contacts. The completed device is shown in cross section in Fig 3. Fig 4 shows electrical characteristics from 100 nm gate length enhancement mode fully self aligned III-V MOSFETs fabricated with the above process flow a significant development towards convergence of III-V MOSFET and silicon VLSI fabrication methodologies.

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[1] http://www.itrs.net/Links/2007ITRS/Home2007.htm
[2] R.J.W. Hill et al., , *IEEE Electron. Dev. Letts.*, 28, pp 1080-1082, 2006.

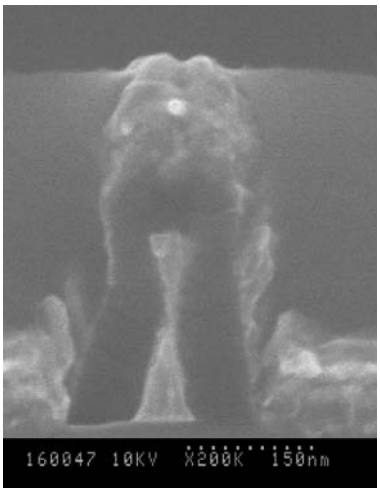

Fig 1. Cross section SEM after dry etch O_2 etch back to expose the ohmic contact metal sitting on top of the gate.

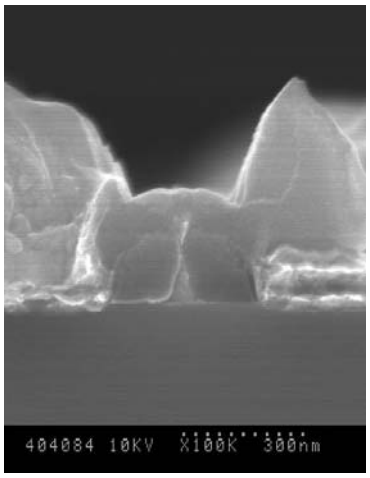

Fig 2. Cross section SEM after $Ar/O_2/SF_6$ reactive ion etch and O_2 dry etch to remove the ohmic contact metal on the gate.

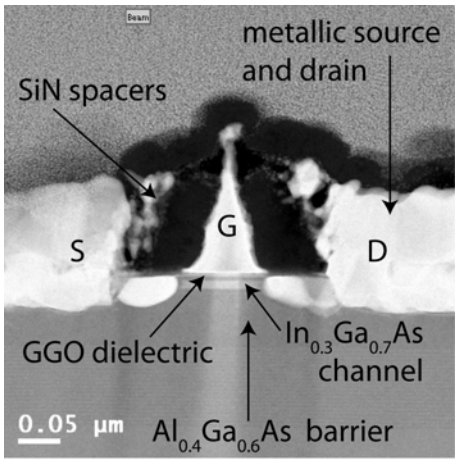

Fig 3. Dark Field STEM cross section of L_g= 100 nm self-aligned device

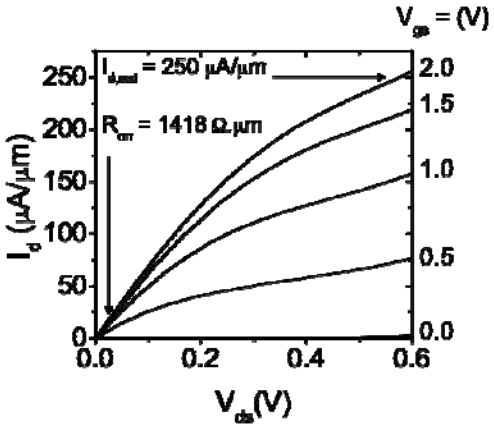

Fig. 4. I_dV_{ds} characteristics of a L_g= 100 nm self-aligned device