MAPPER: HIGH THROUGHPUT MASKLESS LITHOGRAPHY

M.J. Wieland, G. de Boer, G.F. ten Berge, L. Dinu-Gürtler R. Jager, T. van de Peut, J.J.M. Peijster, E. Slot, S.W.H.K. Steenbrink, T.F. Teepen, A.H.V. van Veen, B.J. Kampherbeek , T.Y. Fang*, S.J. Lin*, S.M. Chang*, Faruk Krecinic*, and J.H. Lin*

*Taiwan Semiconductor Manufacturing Company, LTD., 8, Lihsin 6th road, Hsinchu 30077, Taiwan R.O.C.
MAPPER Lithography B.V., Computerlaan 15, 2628 XK Delft, The Netherlands

Maskless electron beam lithography, or electron beam direct write, has been around for a long time in the semiconductor industry and was pioneered from the mid-1960s onwards. This technique has been used for mask writing applications as well as device engineering and in some cases chip manufacturing. However because of its relatively low throughput compared to optical lithography, electron beam lithography has never been the mainstream lithography technology. To extend optical lithography, double patterning, as a bridging technology, and EUV lithography are currently explored. Irrespective of the technical viability of both approaches, one thing seems clear. They will be expensive [1].

Composing of massively parallel electron beams writing with high-speed optical data transportation for switching the electron beams, an optical column can be made with a throughput of 10-20 wafers per hour. By clustering several of these columns together high throughputs up to 100-200 wafers per hour, comparable to the latest optical scanner, can be realized in a small footprint. This enables a highly cost-competitive alternative to double patterning and EUV lithography.

In 2007 the Proof of Lithography milestone was obtained by exposing in the Demonstrator 45-nm half pitch structures with 110 electron beams at 5keV in parallel, where all the beams were individually switched on and off [2]. To verify tool performance in a production environment, multiple tools are being built and integrated with a 300 mm wafer stage. This paper will depict the design of the tools, the status of integration and imaging performance of which some are shown in figures 1 and 2. To ensure that this technology becomes a viable alternative for semiconductor manufacturing at the 22-nm node and beyond, several technical challenges need to be demonstrated, such as for example a clear resolution and throughput roadmap to enable extendibility, solutions for proximity correction, beam-to-beam uniformity and stability, and so on. In this paper we will describe the challenges and our efforts to mitigate these risks.

[1] B. J. Lin, presentation Sematech Lithography workshop 2008, Bolton Landing
[2] E. Slot et al., Proc. of SPIE Vol. 6921, 69211P, (2008)

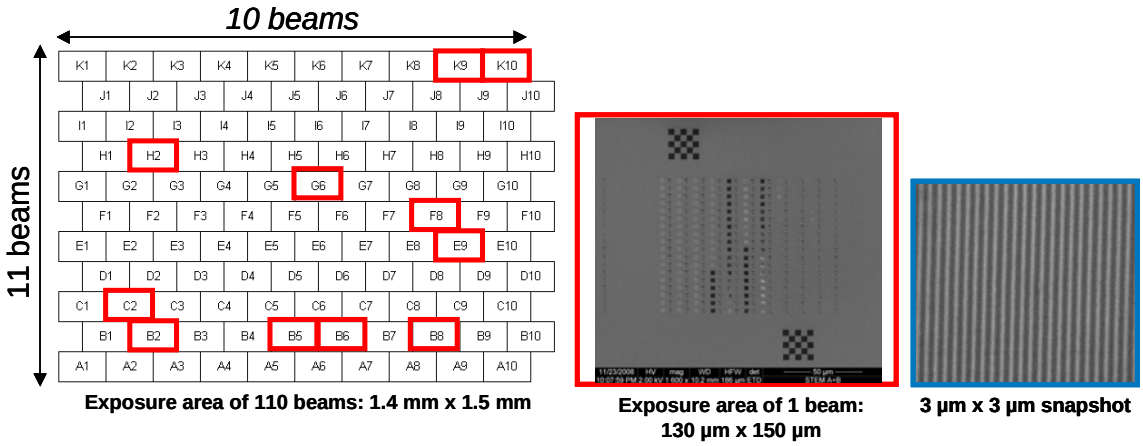

Figure 1 Overview of how the 110 beams are arranged in the slit and what to expose

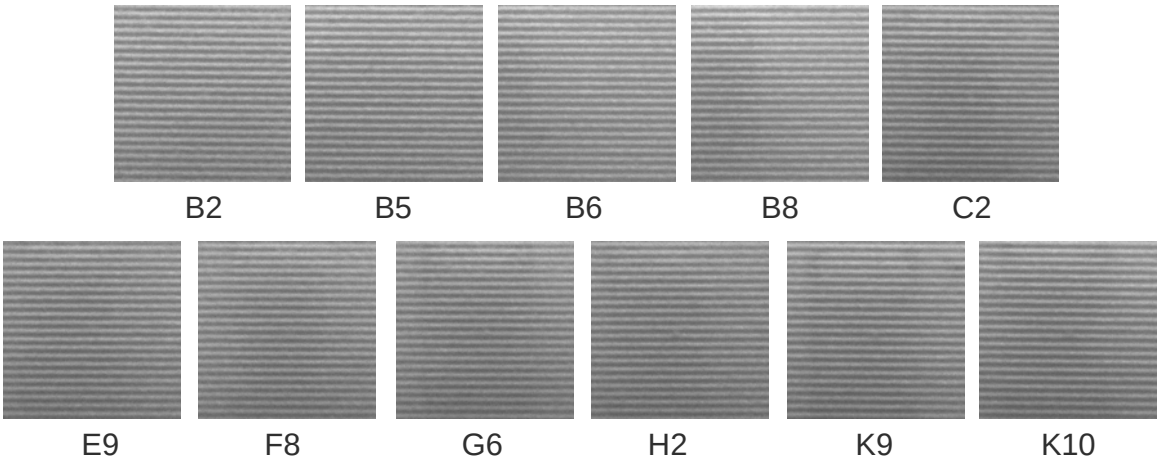

Figure 2 Snapshot of 45 nm half pitch exposures for eleven randomly selected beams