Electrostatic Exfoliation of Pre-Patterned Graphene Micro- and Nanostructures

Xiaogan Liang,* Allan S. P. Chang, Yuegang Zhang, Bruce D. Harteneck,

Hyuck Choo, Deirdre L. Olynick, and Stefano Cabrini

Molecular Foundry, Lawrence Berkeley National Laboratory, 1 Cyclotron Road,

Berkeley, California 94720

Graphene is of great interest as a material for next-generation electronics because of its superior electronic properties.[1] Two of important challenges for scale-up applications are incorporating graphene over large areas[2] and patterning nanostructures to achieve desirable electronic characteristics. Obviously, an approach to simultaneously achieve graphene micro- and nanostructures over large areas would be a benefit to the practical applications of graphene.

We present a novel nanofabrication route, which uses a combination of electrostatic exfoliation with micro and nano lithographically patterned highly oriented pyrolytic graphite (HOPG) to produce pristine graphene features and fabricate electronic devices.[3,4] With this method, we have successfully demonstrated the exfoliation/printing of few-layer-graphene (FLG) features ranging from 18 nm to 100 µm. Furthermore, we have fabricated graphene nanoribbon transistors using patterned graphene nanolines.

Fig. 1 schematically illustrates the electrostatic exfoliation of prepatterned FLG features. Firstly, standard lithographic techniques are used to make raised micro- and nanostructures on the HOPG template. Subsequently, the FLG features are exfoliated from the HOPG template and printed on a Si/SiO_2 substrate by using electrostatic exfoliation.[3]

Fig. 2 shows the scanning electron micrographs (SEMs) of raised features prepatterned on a HOPG template, which includes (a) 5 x 5 µm, 10 x 10 µm periodic squares and 100 x 50 µm rectangles, (b) 1.4 µm size periodic pillars, and (c) 15 nm nanolines.

Fig. 3 shows the representative SEM images of electrically exfoliated FLG features on a Si/SiO_2 substrate, which include (a) 5 x 5 µm periodic squares, (b) 1.4 µm diameter periodic pillars, and (c) 18 nm nanolines with 300 nm spacing.

Fig. 4 (a) shows the SEM image of a back-gated graphene transistor consisting of a 32 nm wide FLG nanoline as the transistor channel. Fig. 4 (b) plots the drain-source current (I_{DS}) as a function of the gate voltage (V_G), from which the hole mobility was extracted to be μ_h = 1,050 cm^2/Vs.

Our electrostatic exfoliation/print process could be repeated to print the pre-patterned pristine graphene nanostructures over wafer-sized areas. The printed graphene features faithfully remain the original pattern and arrangement pre-defined on HOPG templates. Such method could be used for constructing graphene-based integrated circuits in the future.

References

1. Novoselov, K. S.; Geim, A. K.; Morozov, S. V.; Jiang, D.; Zhang, Y.; Dubonos, S. V.; Grigorieva, I. V.; Firsov, A. A. Science **2004**, 306, (5696), 666-669.

2. Liang, X.; Fu, Z.; Chou, S. Y. Nano Letters **2007**, 7, (12), 3840-3844

3. Sidorov, A. N.; Yazdanpanah, M. M.; Jalilian, R.; Ouseph, P. J.; Cohn, R. W.; Sumanasekera, G. U. Nanotechnol. **2007**, 18(13), 135301

4. Liang, X. G.; Chang, A. S. P.; Zhang, Y. G.; Harteneck, B. D.; Choo, H.; Olynick, D. L.; and Cabrini. S, Nano Letters Publication Date (Web): December 10, **2008**

* Email: xliang@lbl.gov

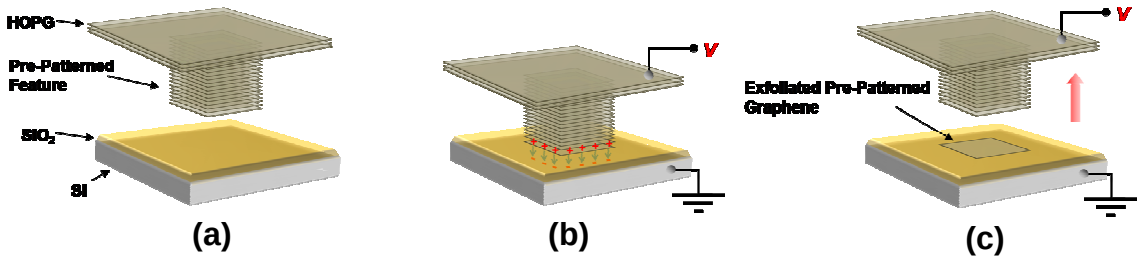

Fig. 1 Schematic of electrostatic exfoliation of pre-patterned graphene. (a) Initial setup with a structured HOPG template, (b) Application of a voltage between the HOPG template and the Si substrate after conformal contact, and (c) Electrostatic exfoliation.

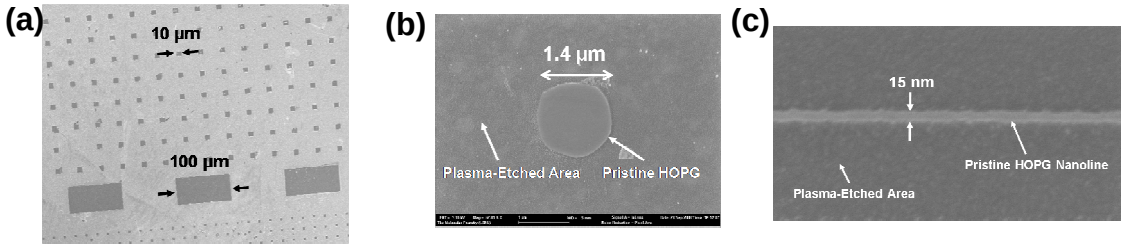

Fig. 2 SEM images of raised features prepatterned on HOPG templates, which includes (a) 5 x 5 µm, 10 x 10 µm, and 100 x 50 µm rectangles, (b) 1.4 µm size pillars, and (c) 15 nm nanolines. Micro- and nanoscale features were patterned by using photolithography and electron beam induced deposition (EBID), respectively, followed with O_2-based RIE.

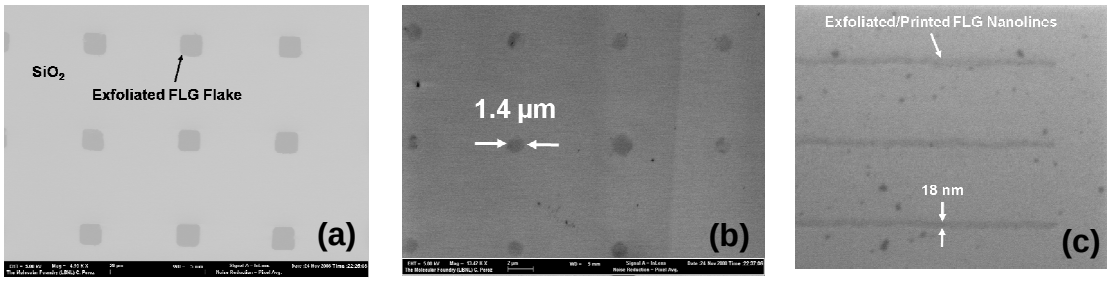

Fig. 3 Representative SEM images of electrically exfoliated/printed few-layer-graphene (FLG) features, which includes (a) 5 x 5 µm squares, (b) 1.4 µm size periodic pillars, and (c) 18 nm wide nanolines.

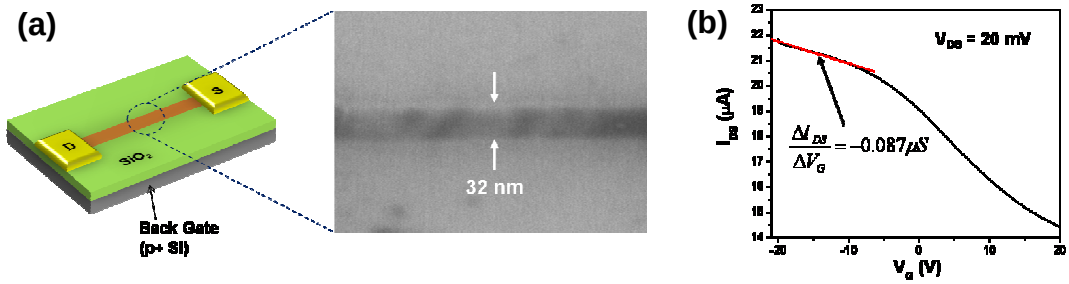

Fig. 4 (a) A back-gated graphene field-effect transistor (GFET) with a 32 nm wide, 0.53 µm long as-exfoliated FLG line as the channel. (b) I_{DS} - V_G of the GFET, from which the hole mobility is extracted to be μ_h = 1,050 cm^2/Vs.

* Email: xliang@lbl.gov